

COMPAL CONFIDENTIAL

MODEL NAME :EDC40  
PCB NO : LA-G871P  
BOM P/N : 431ADY31L0x

Merion 14 AR  
Whiskey lake-U U42  
2019-03-05  
REV : 1.0 (A00)

- @ : Nopop Component
- EMI@ : EMI Component
- @EMI@ : EMI Nopop Component
- ESD@ : ESDComponent
- @ESD@ : ESD Nopop Component
- RF@ : RF Component
- @RF@ : RF Nopop Component
- CONN@ : Connector Component
- CXDP@ : XDP Component
- DS3@ : Deep sleep support
- NDS3@ : non Deep sleep support
- 750@ : NUVOTON NPCT750 TPM Component
- ST33@ : ST ST33HTPH TPM Component
- RTD3@ : RTD3 support
- @RTD3@ : RTD3 Nopop Component
- NRTD3@ : non RTD3 support
- VPRO@ : vPro Component
- NVPRO@ : Non-vPro Component
- JUMP@ : Jump solder and short
- @JUMP@ : Jump no solder
- i7@ : Only i7 config support 4\*4 antenna

Power CKT : Merion 14\_WHL\_PWR\_X02\_1228a  
GPIO map : 20181221a Rev1.5

Part Number	Description
DAA000HW010	PCB 2EE LA-G871P REV1 MB AR 1


Layout Dell logo



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REV:A00  
PWB:7YM2P

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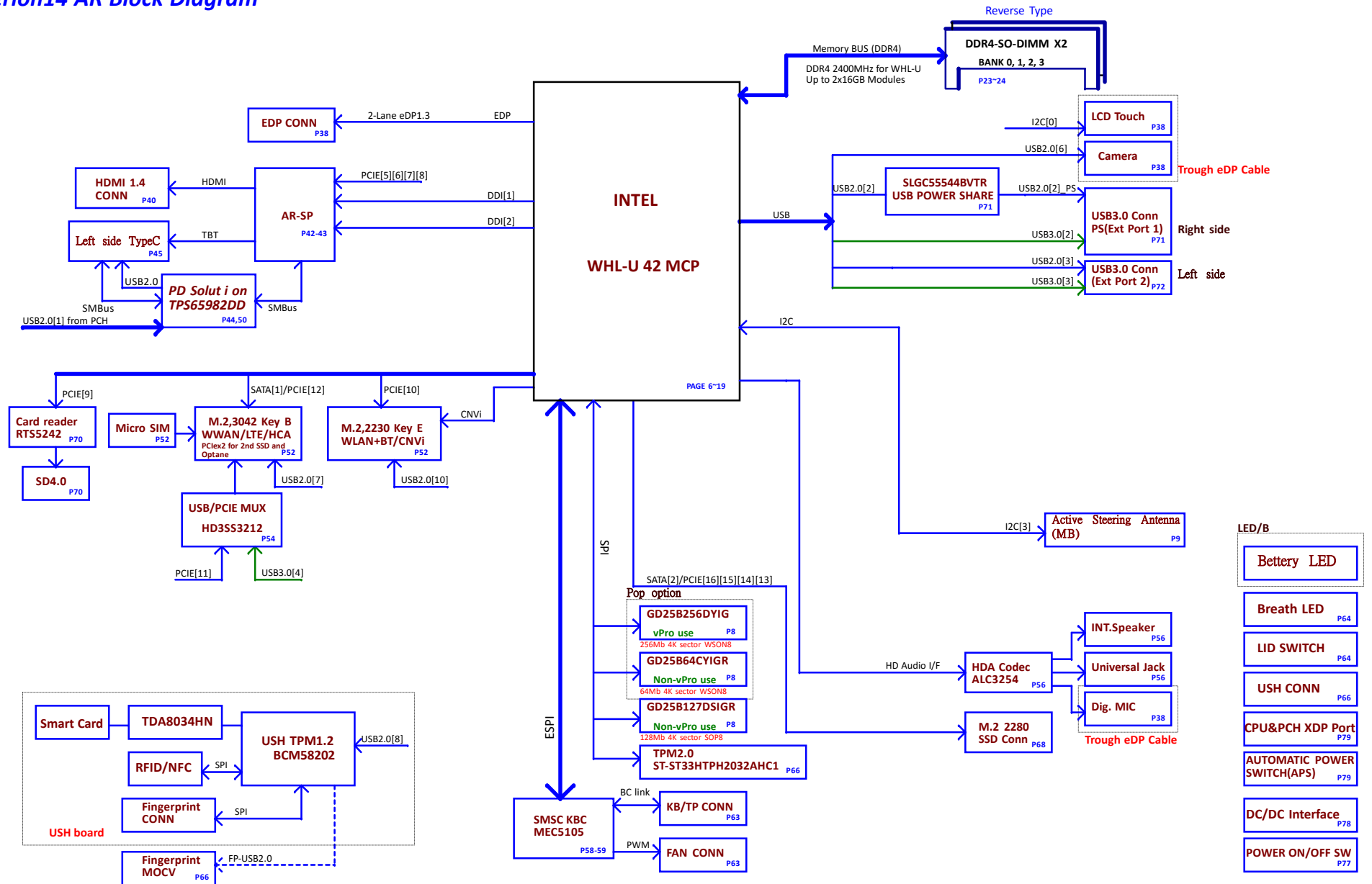
Title

Cover Sheet

SizeDocument NumberRev1.0

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# Merion14 AR Block Diagram



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Block Diagram

LA-G871P

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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1		PCIE-1		N/A
USB3.0-2		PCIE-2		JUSB1-->Right
USB3.0-3		PCIE-3		JUSB2-->Left
USB3.0-4		PCIE-4		M.2 3042(LTE)
USB3.0-5		PCIE-5		Alpine Ridge - SP
USB3.0-6		PCIE-6		
		PCIE-7		
		PCIE-8		
		PCIE-9		Card Reader
		PCIE-10		M.2 2230(WLAN)
		PCIE-11	SATA-0	M.2 3042(LTE)
		PCIE-12	SATA-1	
		PCIE-13		M.2 2280 SSD (PCIex4 or SATA)
		PCIE-14		
		PCIE-15	SATA-1*	
		PCIE-16	SATA-2	

USB PORT#	DESTINATION
1	Type C
2	JUSB1-->Right
3	JUSB2-->Left
4	N/A
5	N/A
6	Camera
7	M2 3042(WWAN)
8	USH
9	Reserve for FPR in PB
10	M.2 2230(BT)

PM TABLE

State \ power plane	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_PRIM	+1.2V_MEM +2.5V_MEM +1.0V_VCCSTG	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.8V_RUN
S0	ON	ON	ON
S5 S4/AC	ON	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF

Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL U PCH-LP

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	PCIE* #7	PCIE* #8	PCIE* #9	PCIE* #10	PCIE* #11	PCIE* #12	PCIE* #13	PCIE* #14	PCIE* #15	PCIE* #16
	PCIE* #1	PCIE* #2	PCIE* #3	PCIE* #4	PCIE* #5	PCIE* #6	GbE	GbE	GbE		SATA 0	SATA 1a		GbE	SATA 1b	SATA 2
Intel® RST Support	No Support			No Support			Yes			Yes			Yes			

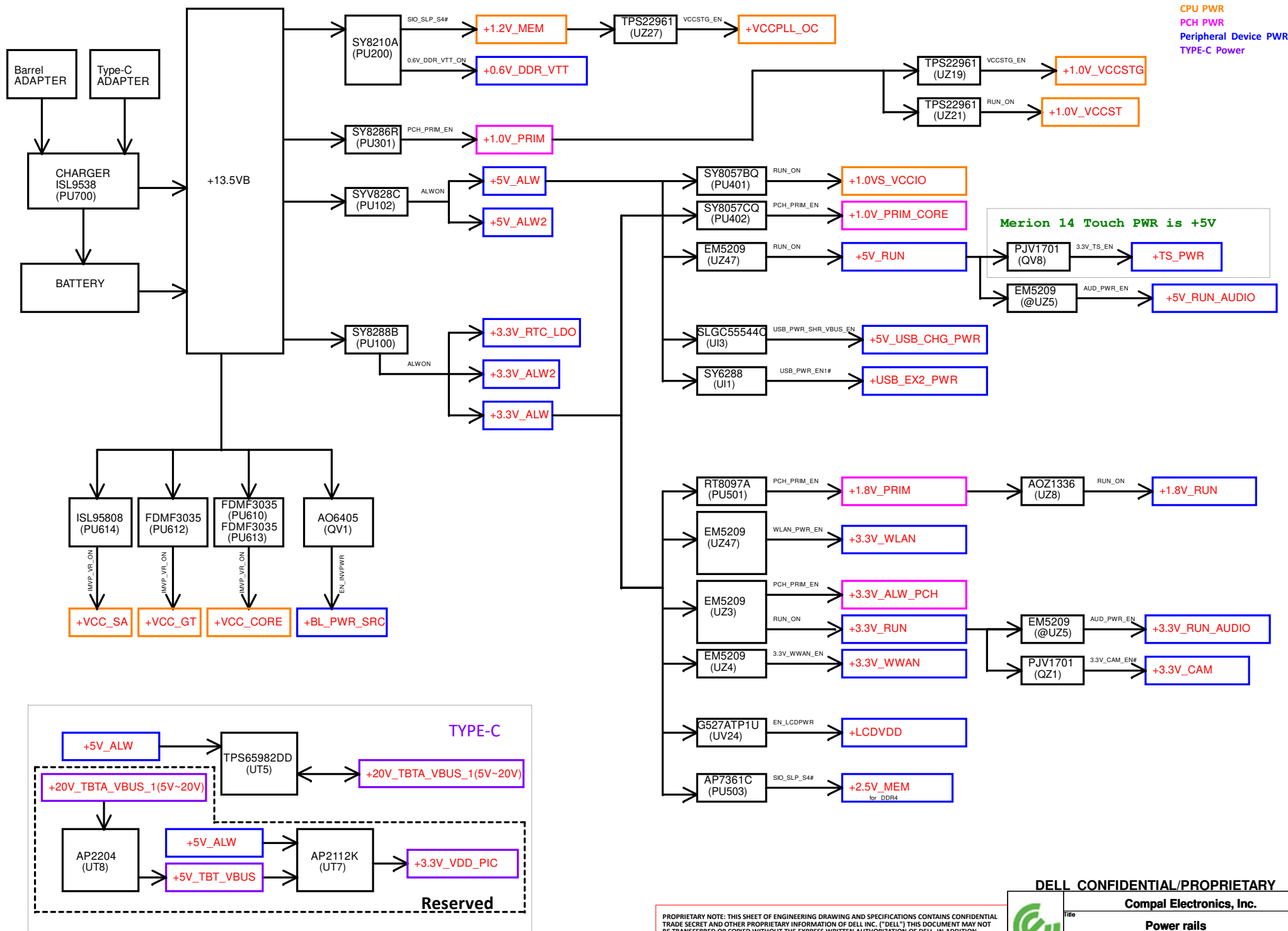
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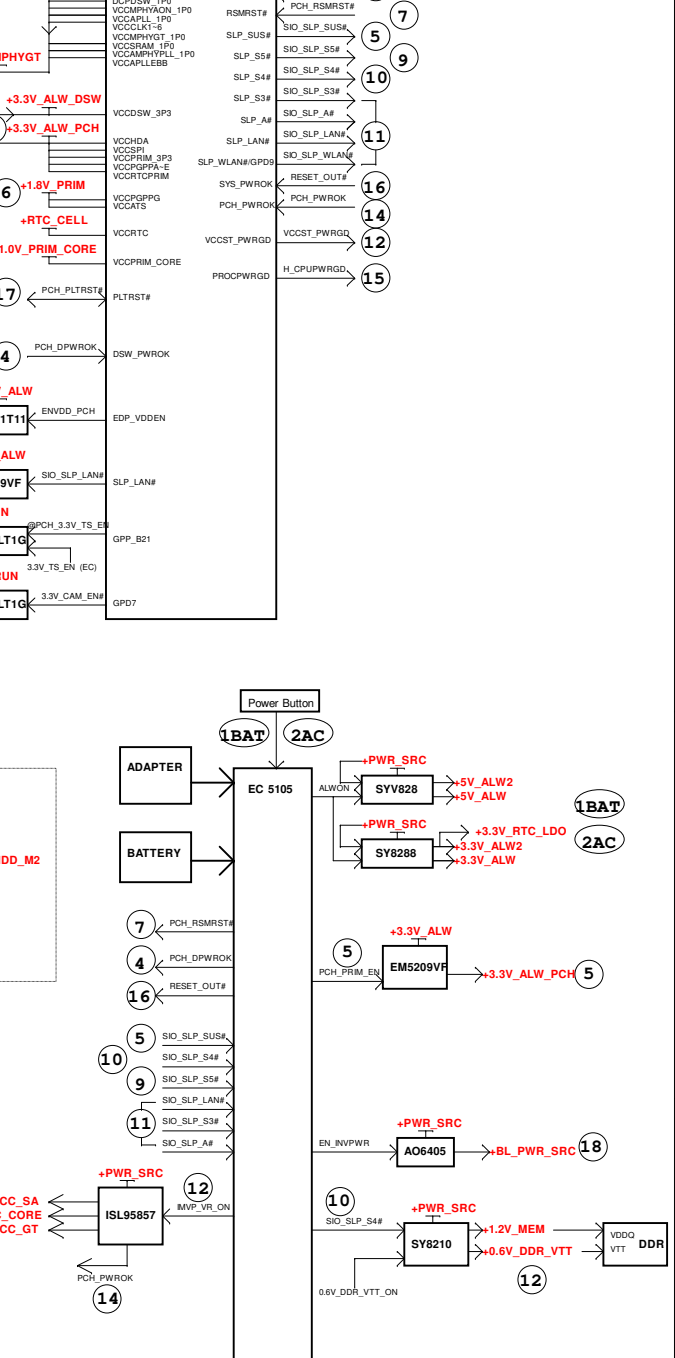
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Figure 10 shows the PCH PWRBTN# pin connection. The PCH block has three pins: VCCPRIM\_1P0, VCCPRIM\_CORE, and PWRBTN#. The PWRBTN# pin is connected to a +1.0V PRIM source and a circular symbol containing the number 8.



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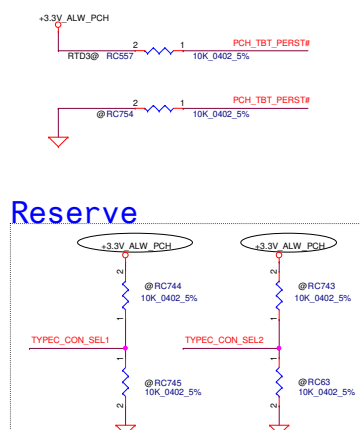
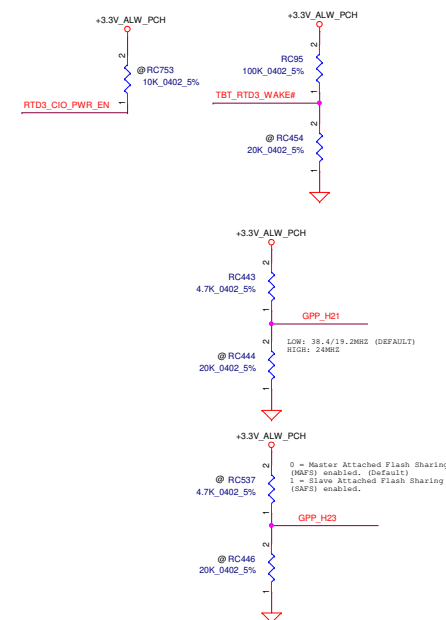
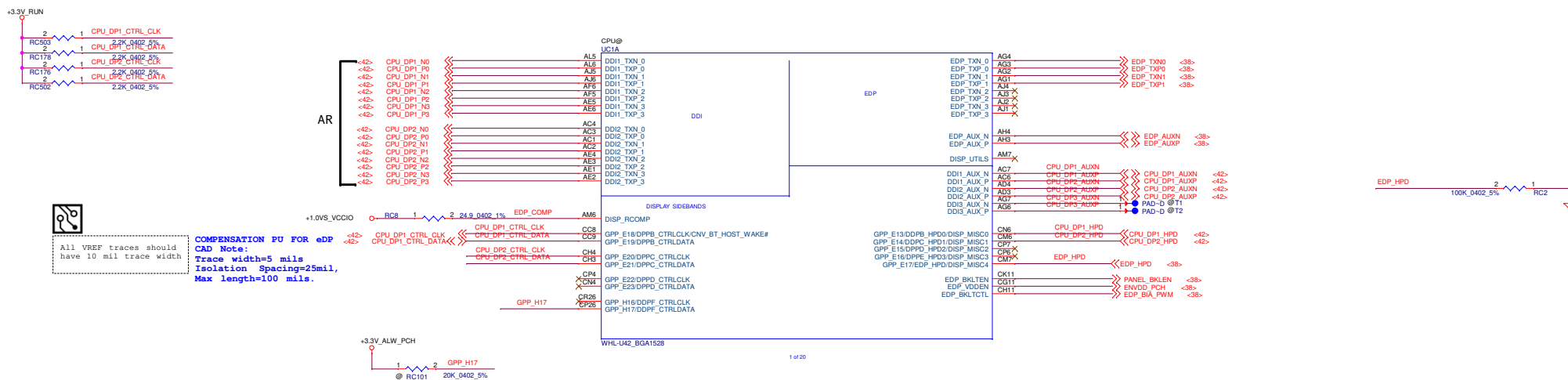
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For 2LANE EDP



Vendor	JAE	FOXCON	TBD	TBD
TYPECON_SEL1	LOW	LOW	HIGH	HIGH
TYPECON_SEL2	LOW	HIGH	LOW	HIGH

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CPU(1/14)DDI,EDP,CSI2,EMMC

LA-G871P

Rev	1.0
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LA-G67 IF

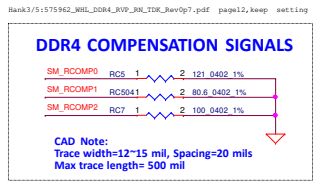
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DDR4, Ballout for side by side(Non-Interleave)



DDR A DQ	A26	DDR0 DQ 0/DDR0 DQ 0	V32	DDR A CLK#0	DDR A CLK#0	<23>
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DDR A DQ	AR18	DDR0 DQ 56/DDR0 DQ 56	W35	DDR A BA3	DDR A BA3	<23>
DDR A DQ	AR17	DDR0 DQ 57/DDR0 DQ 57	W35	DDR A BA3	DDR A BA3	<23>
DDR A DQ	AR16	DDR0 DQ 58/DDR0 DQ 58	W35	DDR A BA3	DDR A BA3	<23>
DDR A DQ	AR15	DDR0 DQ 59/DDR0 DQ 59	W35	DDR A BA3	DDR A BA3	<23>
DDR A DQ	AR14	DDR0 DQ 60/DDR0 DQ 60	W35	DDR A BA3	DDR A BA3	<23>
DDR A DQ	AR13	DDR0 DQ 61/DDR0 DQ 61	W35	DDR A BA3	DDR A BA3	<23>
DDR A DQ	AR12	DDR0 DQ 62/DDR0 DQ 62	W35	DDR A BA3	DDR A BA3	<23>
DDR A DQ	AR11	DDR0 DQ 63/DDR0 DQ 63	W35	DDR A BA3	DDR A BA3	<23>



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CPU(2/14)DDR4

LA-G871P

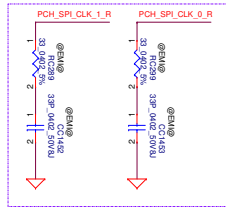
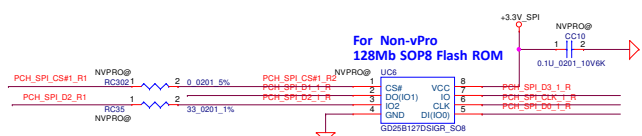
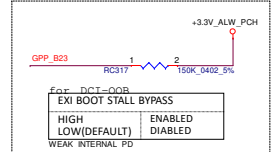
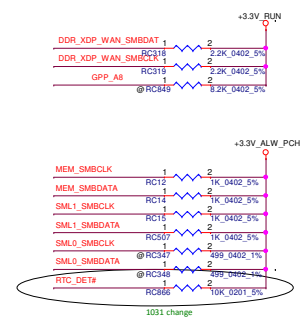
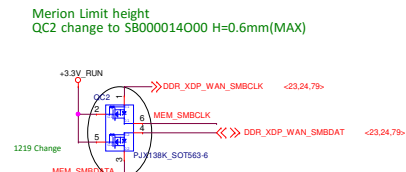
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Date: Tuesday, March 05, 2019

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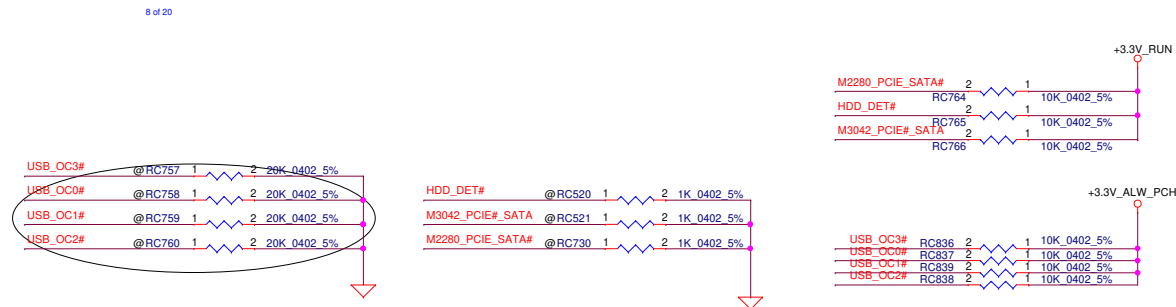
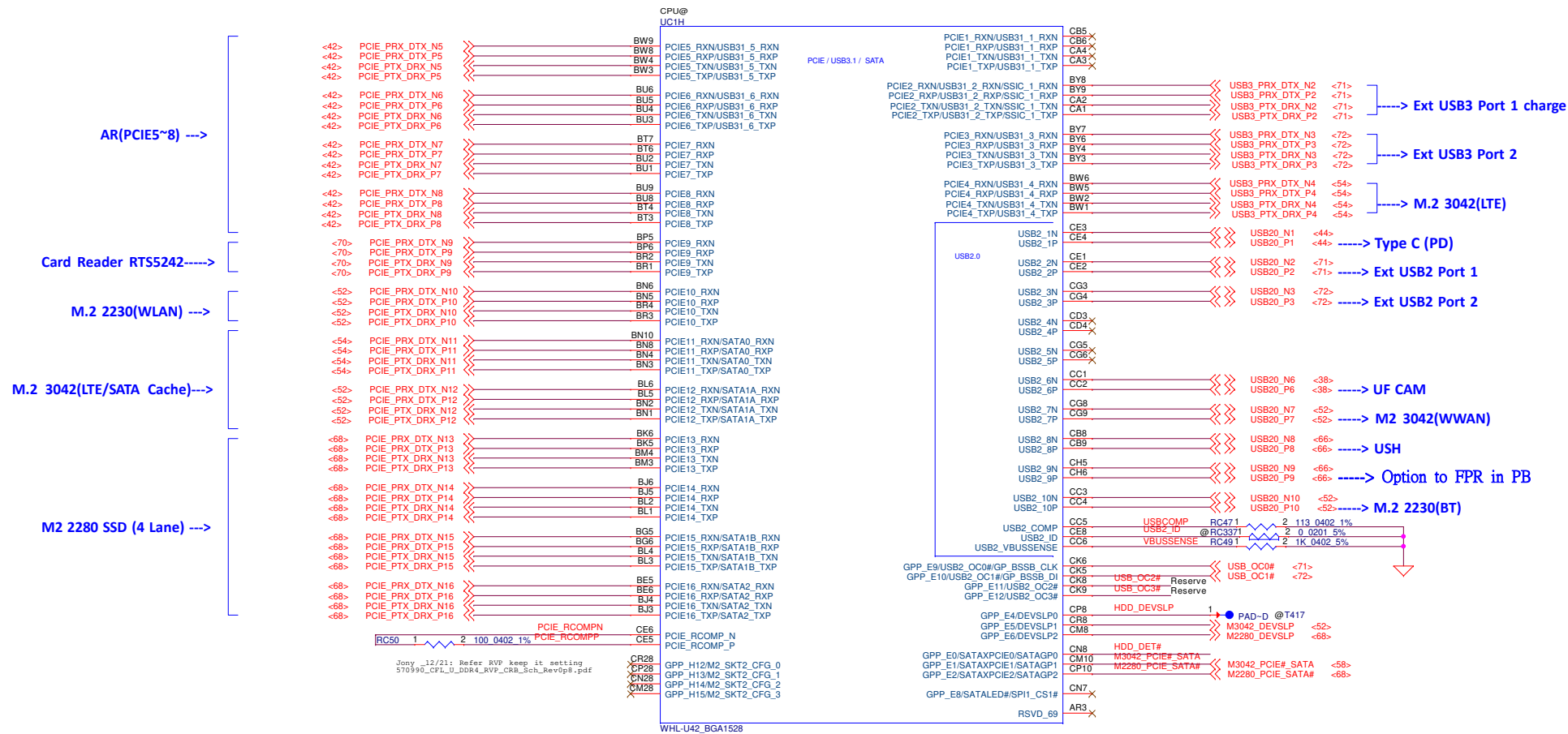








# For Merion AR (follow WHL 180416a port map)



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Compal Electronics, Inc.

Title			
CPU(5/14)PCIE,USB,SATA			
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M.2 3042 WWAN-->

M.2 2230 WLAN-->

M.2 2280 SSD-->

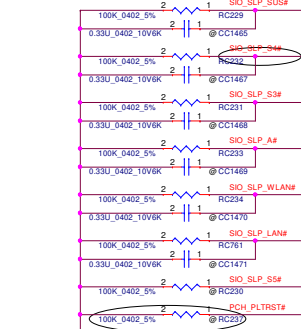
Card Reader -->

AR-->

+3.3V\_ALW\_DSW

+1.0V\_VCCST

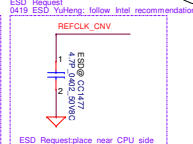
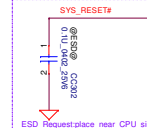
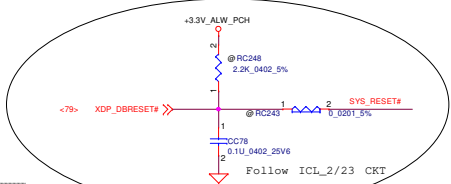
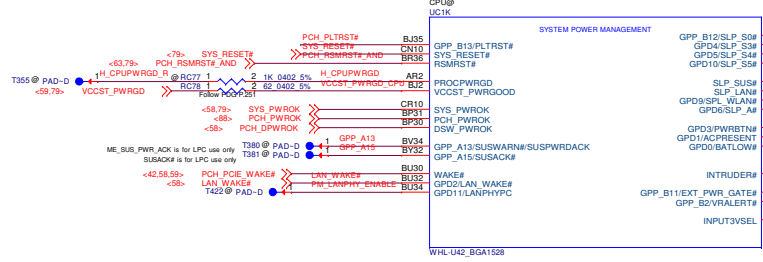
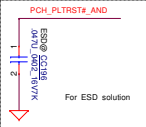
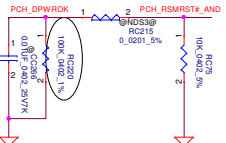
PCH GLITCH ISSUE MITIGATION(PDG p.130)



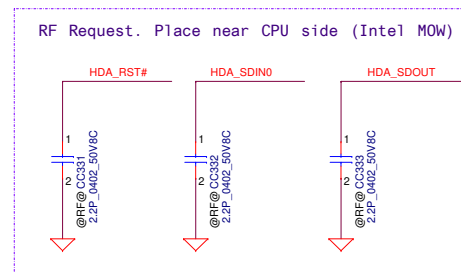
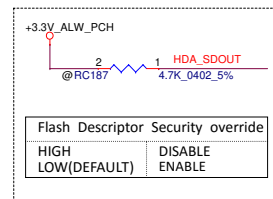
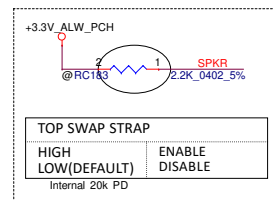
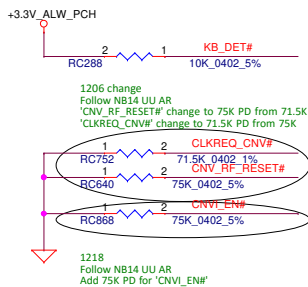
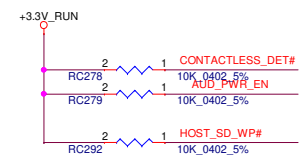
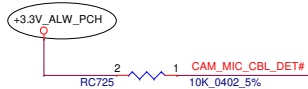
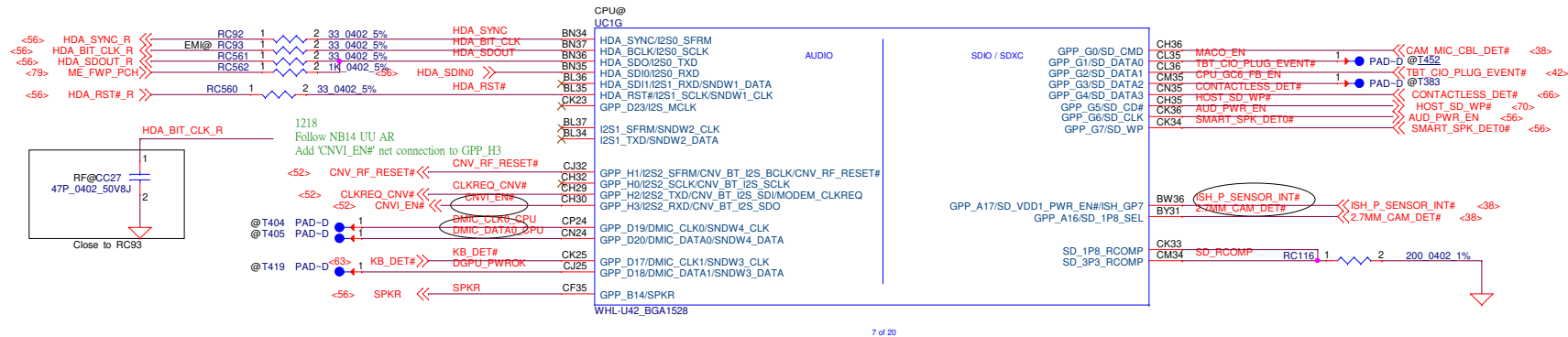
T211 change  
Follow NB14 UU AR, Intel CNV1 recommendation RC237 pop.  
But measure cold reset and Global reset sequence timing fail, So depop RC237



RC215  
POP  
DE-POP



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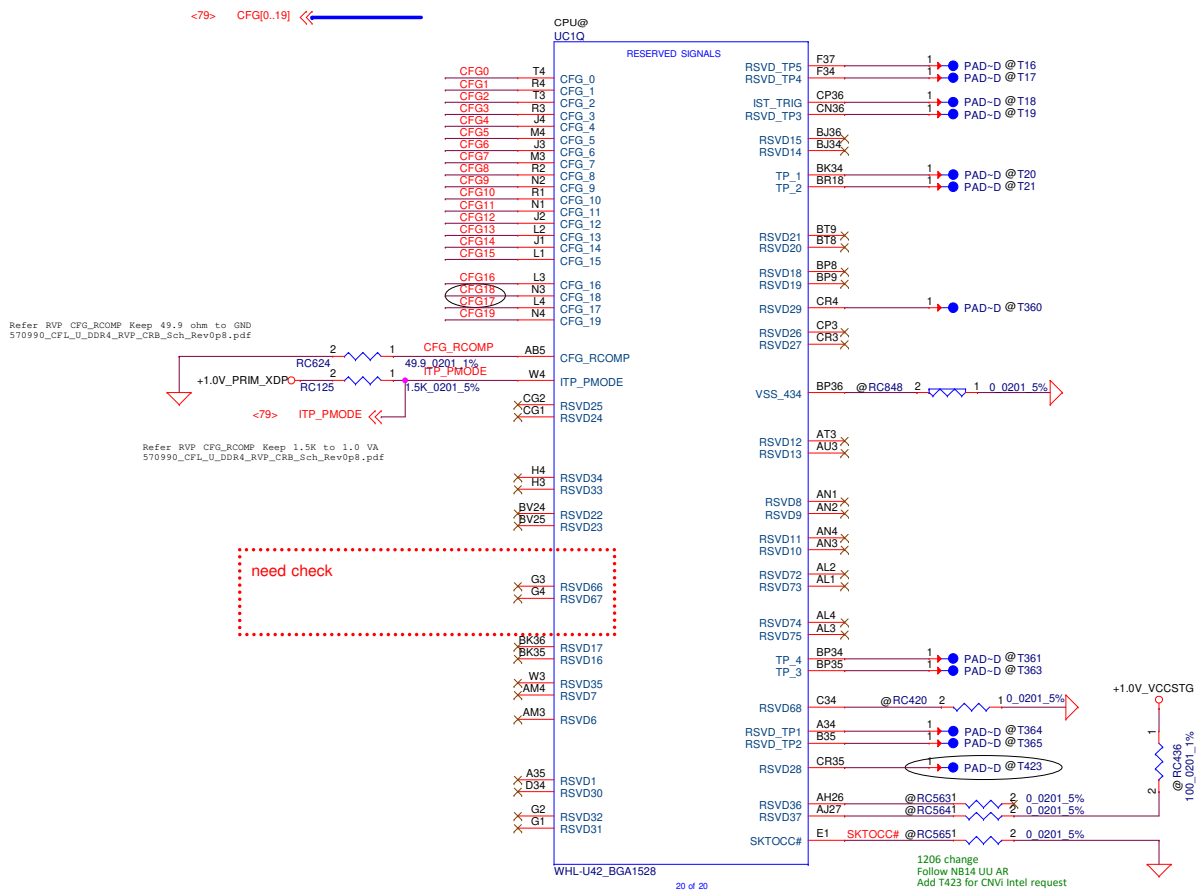
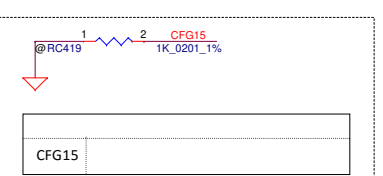
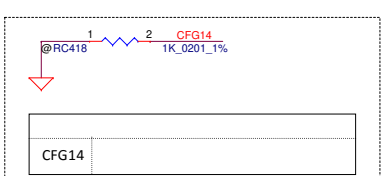
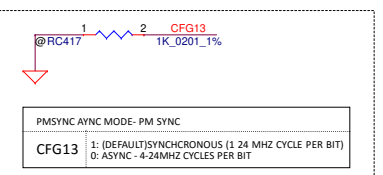
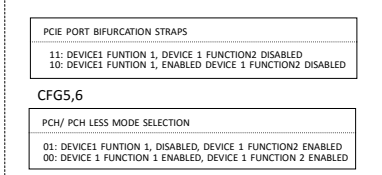
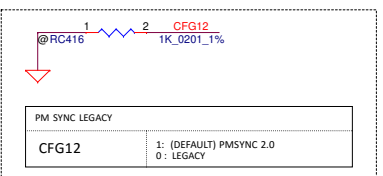
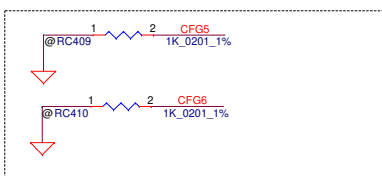
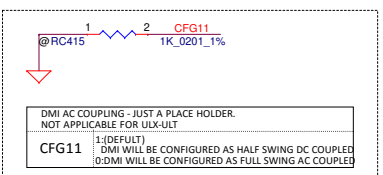
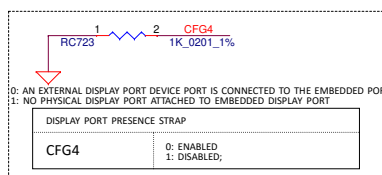
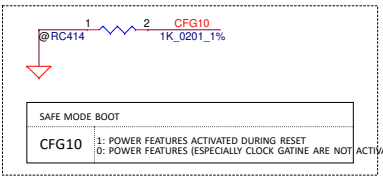
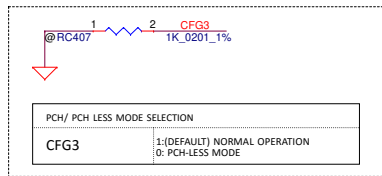
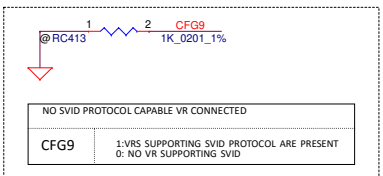
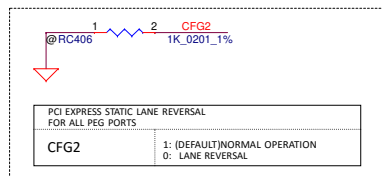
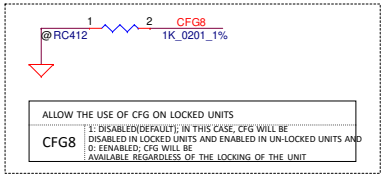
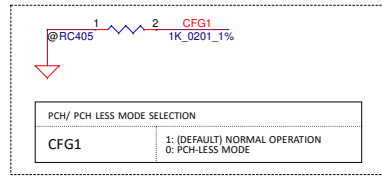
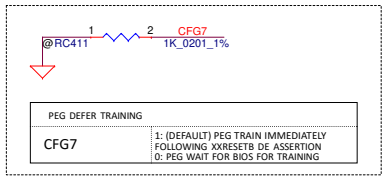
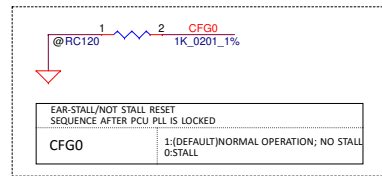


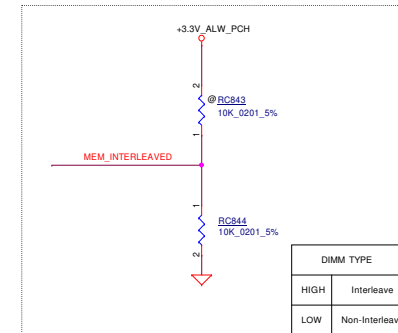
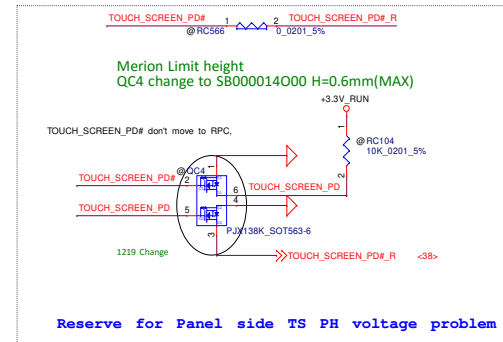
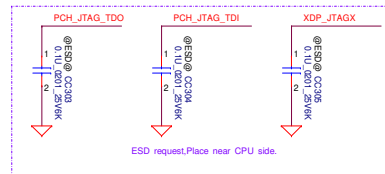
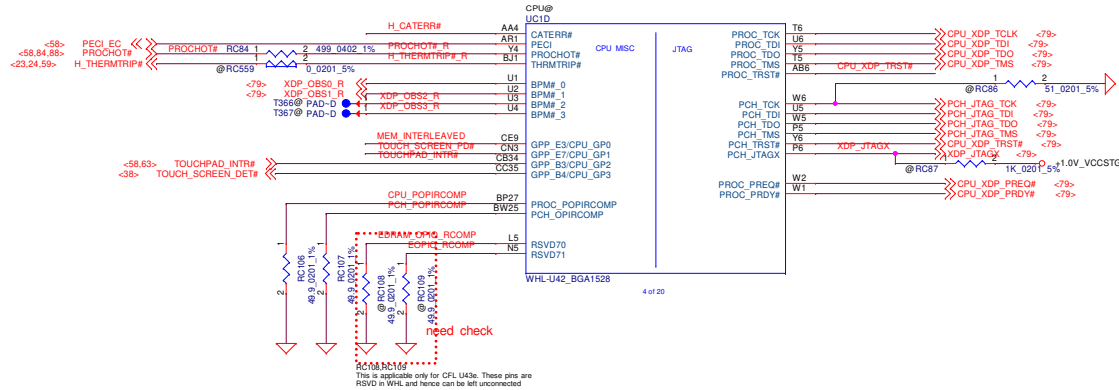
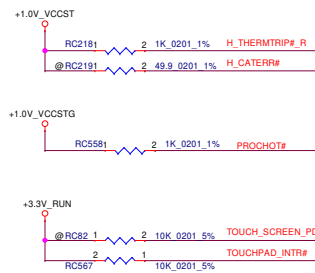
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Compal Electronics, Inc.			
Title			
CPU(7/14)MISC,JTAG,HDA,SDIO			
Size	Document Number	Rev	
	LA-G871P	1.0	
Date	Tuesday, March 05, 2019	Sheet	12 of 109

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CPU(9/14)XDP			
File	Document Number	LA-G871P	Rev 1.0
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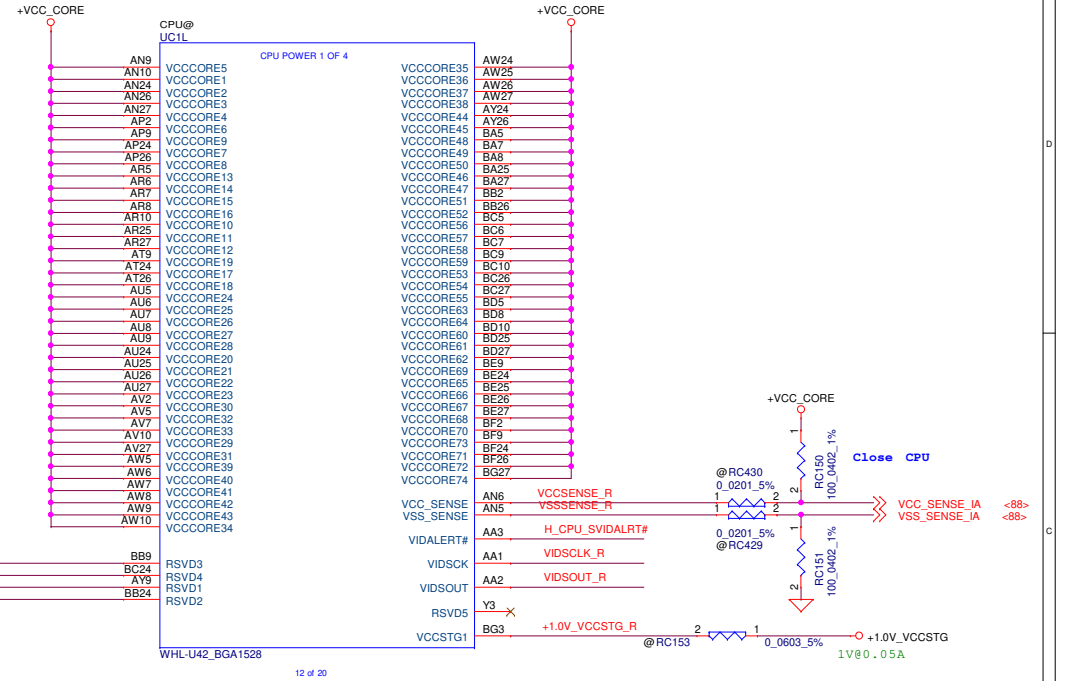
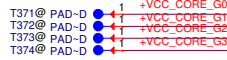
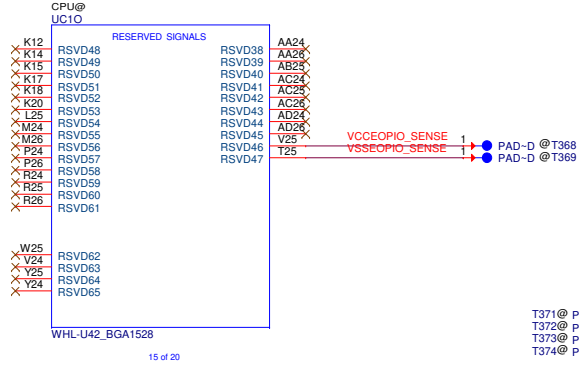
PSC(Primary side cap) : Place as close to the package as possible  
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:  
Package edge > 0402 caps > 0805 caps > Bulk caps > Power source

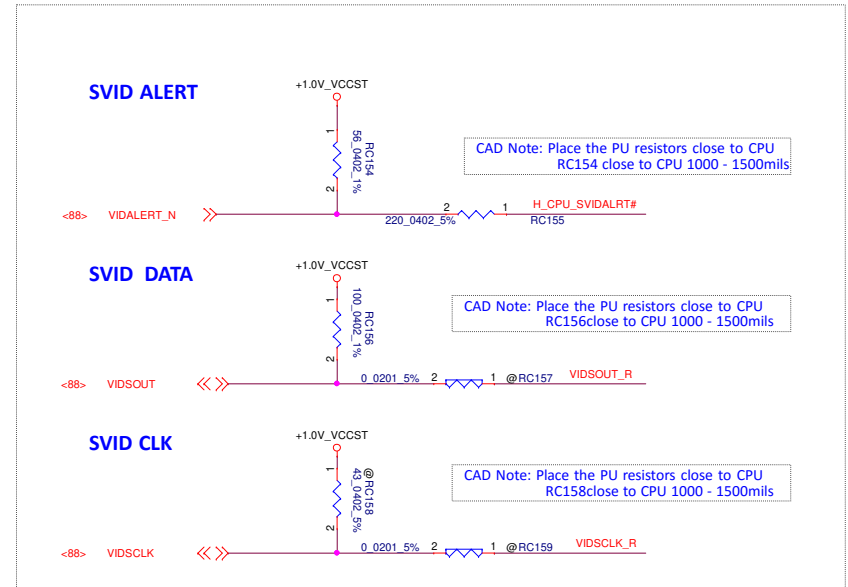
+VCC\_CORE: 0.55~1.5V, 29A  
+VCC\_EDRAM: 1V, 2.5A

+V1.8S\_EDRAM: 1.8V, 50mA - REMOVE  
+VCC\_EOPIO: 0.8~1V, 2A - REMOVE

Pin Number	CPU U43e	WHL U42 Q5/Production	CPU U22/WHL U42 ESO/1
AH26	ZVMH	RSVD	RSVD
T25	VSS_EOPIO_SENSE	RSVD	RSVD
V25	VCC_EOPIO_SENSE	RSVD	RSVD
AA24	VCC_EOPIO	RSVD	RSVD
AA26	VCC_EOPIO	RSVD	RSVD
AA28	VCC_EOPIO	RSVD	RSVD
AA29	VCC_EOPIO	RSVD	RSVD
AA30	VCC_EOPIO	RSVD	RSVD
AA31	VCC_EOPIO	RSVD	RSVD
AA32	VCC_EOPIO	RSVD	RSVD
AA33	VCC_EOPIO	RSVD	RSVD
AA34	VCC_EOPIO	RSVD	RSVD
AA35	VCC_EOPIO	RSVD	RSVD
AA36	VCC_EOPIO	RSVD	RSVD
AA37	VCC_EOPIO	RSVD	RSVD
AA38	VCC_EOPIO	RSVD	RSVD
AA39	VCC_EOPIO	RSVD	RSVD
AA40	VCC_EOPIO	RSVD	RSVD
AA41	VCC_EOPIO	RSVD	RSVD
AA42	VCC_EOPIO	RSVD	RSVD
AA43	VCC_EOPIO	RSVD	RSVD
AA44	VCC_EOPIO	RSVD	RSVD
AA45	VCC_EOPIO	RSVD	RSVD
AA46	VCC_EOPIO	RSVD	RSVD
AA47	VCC_EOPIO	RSVD	RSVD
AA48	VCC_EOPIO	RSVD	RSVD
AA49	VCC_EOPIO	RSVD	RSVD
AA50	VCC_EOPIO	RSVD	RSVD
AA51	VCC_EOPIO	RSVD	RSVD
AA52	VCC_EOPIO	RSVD	RSVD
AA53	VCC_EOPIO	RSVD	RSVD
AA54	VCC_EOPIO	RSVD	RSVD
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AA62	VCC_EOPIO	RSVD	RSVD
AA63	VCC_EOPIO	RSVD	RSVD
AA64	VCC_EOPIO	RSVD	RSVD
AA65	VCC_EOPIO	RSVD	RSVD
AA66	VCC_EOPIO	RSVD	RSVD
AA67	VCC_EOPIO	RSVD	RSVD
AA68	VCC_EOPIO	RSVD	RSVD
AA69	VCC_EOPIO	RSVD	RSVD
AA70	VCC_EOPIO	RSVD	RSVD
AA71	VCC_EOPIO	RSVD	RSVD
AA72	VCC_EOPIO	RSVD	RSVD
AA73	VCC_EOPIO	RSVD	RSVD
AA74	VCC_EOPIO	RSVD	RSVD
AA75	VCC_EOPIO	RSVD	RSVD
AA76	VCC_EOPIO	RSVD	RSVD
AA77	VCC_EOPIO	RSVD	RSVD
AA78	VCC_EOPIO	RSVD	RSVD
AA79	VCC_EOPIO	RSVD	RSVD
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AA83	VCC_EOPIO	RSVD	RSVD
AA84	VCC_EOPIO	RSVD	RSVD
AA85	VCC_EOPIO	RSVD	RSVD
AA86	VCC_EOPIO	RSVD	RSVD
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AA97	VCC_EOPIO	RSVD	RSVD
AA98	VCC_EOPIO	RSVD	RSVD
AA99	VCC_EOPIO	RSVD	RSVD
AA100	VCC_EOPIO	RSVD	RSVD



VCCOPC,VCCOPC\_1P8,VCC\_EOPIO for SKYLAKE-U 2+3e  
(w/ on package cache)



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Compal Electronics, Inc.

CPU(10/14)PWR-VCC CORE

LA-G871P

Rev 1.0

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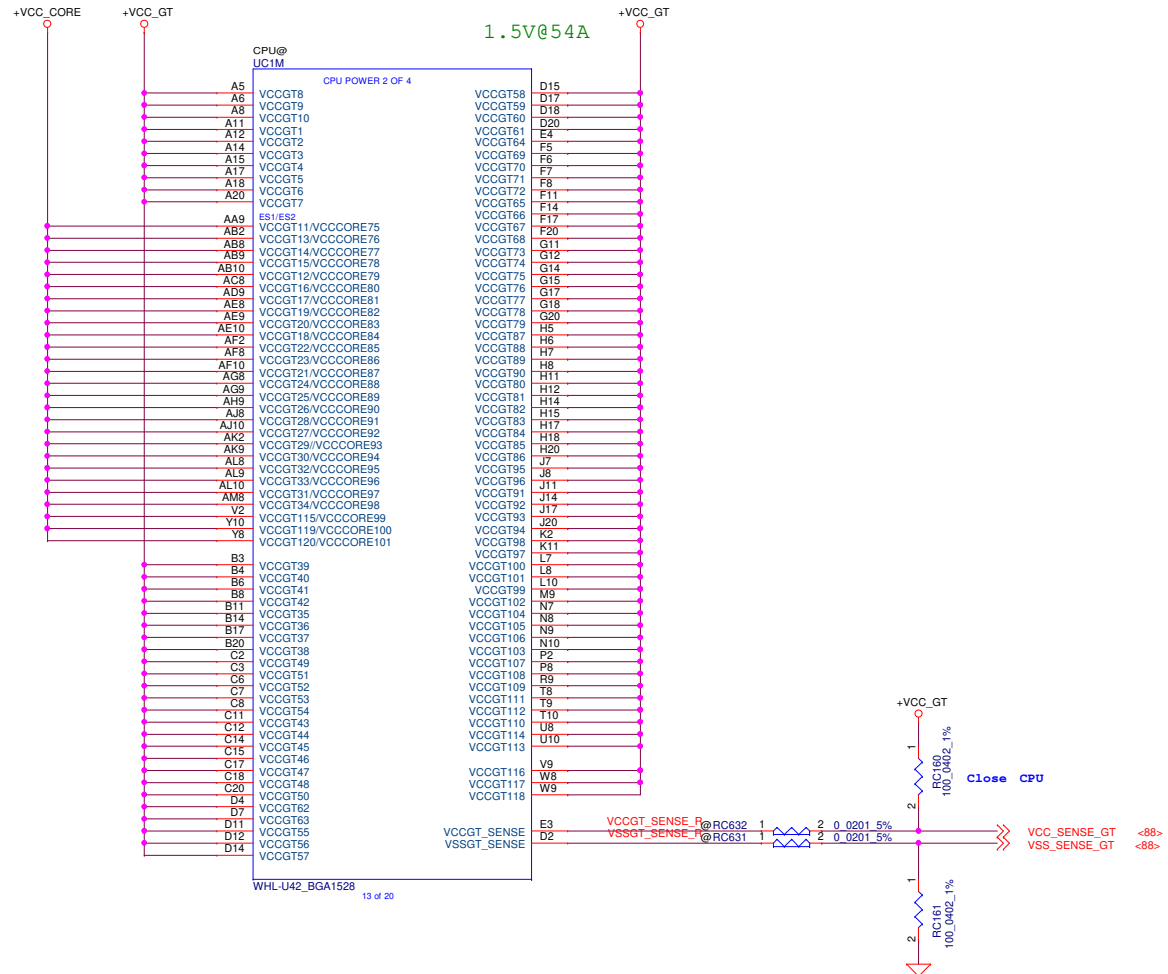
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# THE BALLOUT ONLY FOR WHL ES2 CPU

+VCCGT: 0.55~1.5V, 54A  
+VCCGTX : 0.55~1.5V, 7A

Pin Number	CFL-U43E	WHL ES1 Netname	WHL ES2 Netname
AA9	VCCGT	VCCGT	VCCCGT
AB10	VCCGT	VCCGT	VCCCGT
AB2	VCCGT	VCCGT	VCCCGT
AB8	VCCGT	VCCGT	VCCCGT
AB9	VCCGT	VCCGT	VCCCGT
AC8	VCCGT	VCCGT	VCCCGT
AD9	VCCGT	VCCGT	VCCCGT
AE10	VCCGT	VCCGT	VCCCGT
AE8	VCCGT	VCCGT	VCCCGT
AE9	VCCGT	VCCGT	VCCCGT
AF10	VCCGT	VCCGT	VCCCGT
AF2	VCCGT	VCCGT	VCCCGT
AF8	VCCGT	VCCGT	VCCCGT
AG8	VCCGT	VCCGT	VCCCGT
AG9	VCCGT	VCCGT	VCCCGT
AH9	VCCGT	VCCGT	VCCCGT
AJ10	VCCGT	VCCGT	VCCCGT
AJ8	VCCGT	VCCGT	VCCCGT
AK2	VCCGT	VCCGT	VCCCGT
AK9	VCCGT	VCCGT	VCCCGT
AL10	VCCGT	VCCGT	VCCCGT
AL8	VCCGT	VCCGT	VCCCGT
AL9	VCCGT	VCCGT	VCCCGT
AM8	VCCGT	VCCGT	VCCCGT
V2	VCCGT	VCCGT	VCCCGT
Y10	VCCGT	VCCGT	VCCCGT
Y8	VCCGT	VCCGT	VCCCGT



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Compal Electronics, Inc.

CPU(11/14)PWR-VCCGT

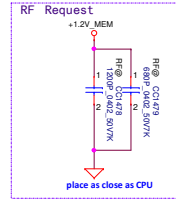
LA-G871P

Rev 1.0

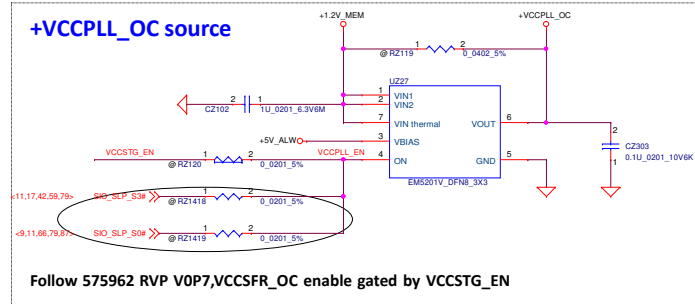
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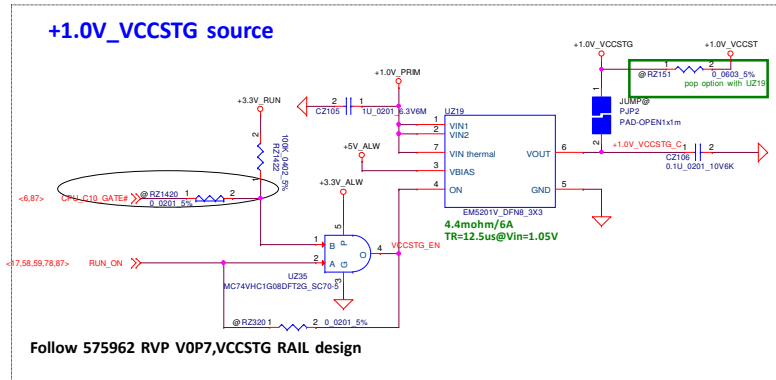
+1.2V\_DDR: 1.2V, 3.5A  
+1.0V\_VCCST: 1V, 120mA; VCCPLL: 1V, 120mA  
+1.0V\_VCCSTG: 1V, 40mA  
+VCCPLL\_OC: 1.2V, 260mA  
+1.0V\_VCCIO: 0.85~0.95V, 3.1A  
+VCC\_SA: 1.15V, 5.1A



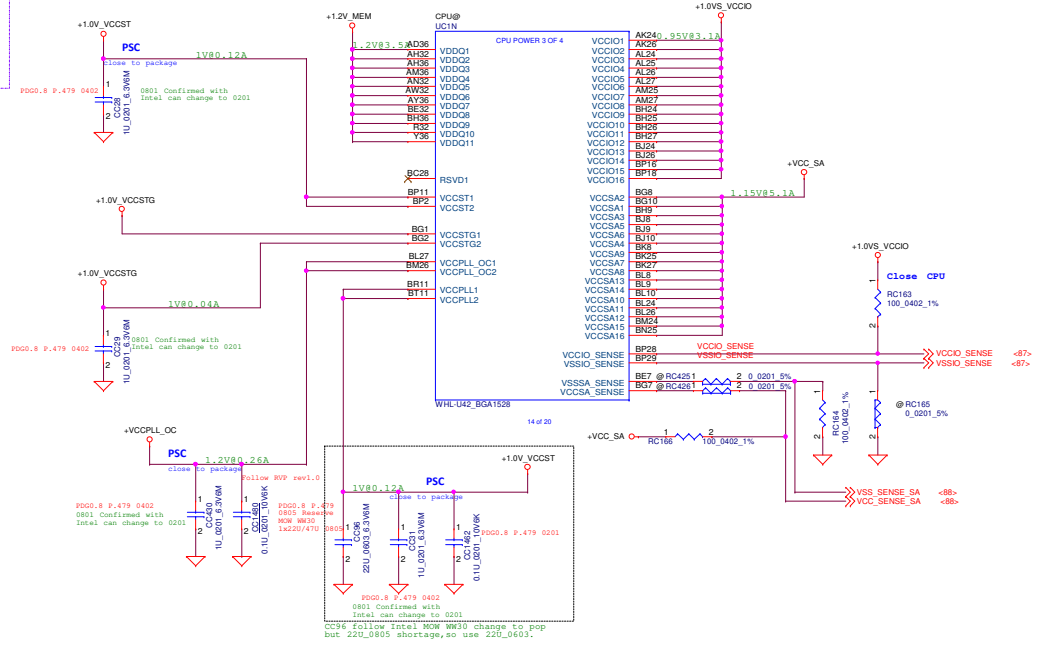
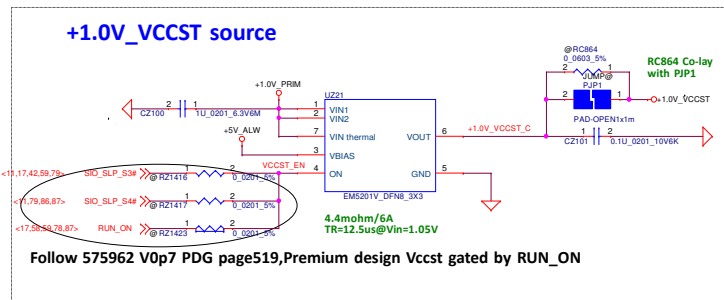
### +VCCPLL\_OC source



### +1.0V\_VCCSTG source



### +1.0V\_VCCST source



WHL U PDG rev0.8 P.479

VDDQ:  
Primary Side cap  
1x 22uF 0603 + 6x 10uF 0402

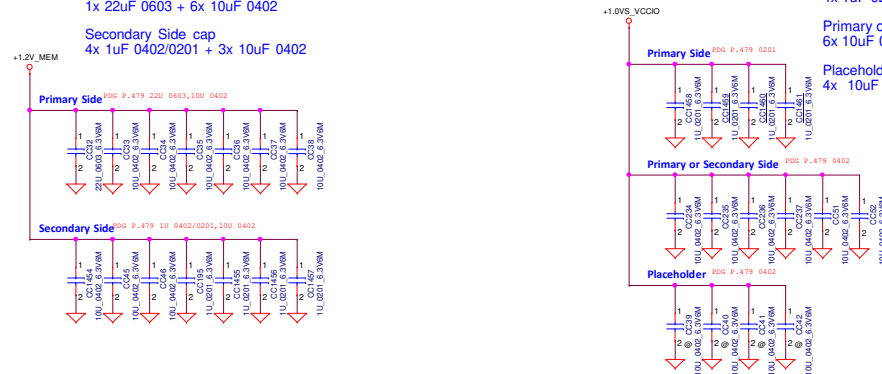
Secondary Side cap  
4x 1uF 0402/0201 + 3x 10uF 0402

WHL U PDG rev0.8 P.479

VCCIO:  
Primary Side cap  
4x 1uF 0201

Primary or Secondary Side  
6x 10uF 0402

Placeholder Only  
4x 10uF 0402



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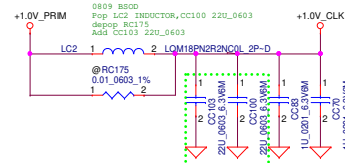
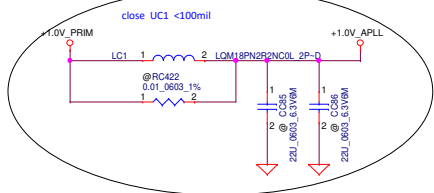


CU(12/14)PWR-VCCIO, MEM

LA-G871P

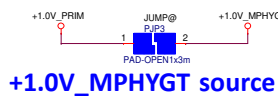
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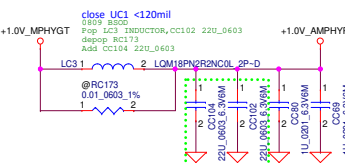


CC100/CC103 one is close to the CPU and the other is far from the CPU.

CC83/CC70 close to CP5



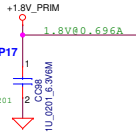
+1.0V\_MPHYGT source



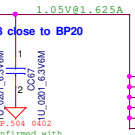
CC102/CC104 one is close to the CPU and the other is far from the CPU.

CC80/CC69 close to BV2

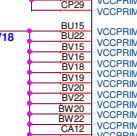
CC98 close to CP17



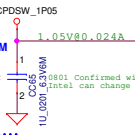
CC67/CC68 close to BP20



CC66 close to BV18

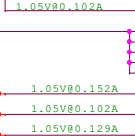


PCH Internal VRM close to BT24

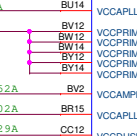


PDG rev0.8 P.509 Place an 22uF edge cap not more than 12 mm away measuring from package edge.

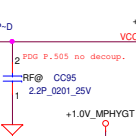
CC1463 close to BR24



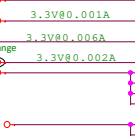
CC1464 close to CP23



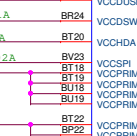
CC80/CC69 close to BV2



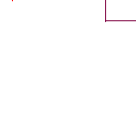
CC1463 close to BR24



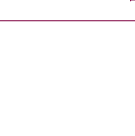
CC1464 close to CP23



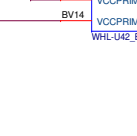
CC80/CC69 close to BV2



CC1463 close to BR24



CC1464 close to CP23



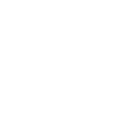
CC80/CC69 close to BV2



CC1463 close to BR24



CC1464 close to CP23



CC80/CC69 close to BV2



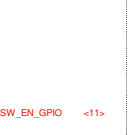
CC1463 close to BR24



CC1464 close to CP23



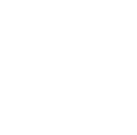
CC80/CC69 close to BV2



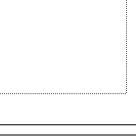
CC1463 close to BR24



CC1464 close to CP23



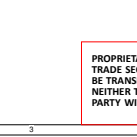
CC80/CC69 close to BV2



CC1463 close to BR24



CC1464 close to CP23



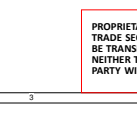
CC80/CC69 close to BV2



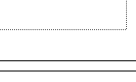
CC1463 close to BR24



CC1464 close to CP23



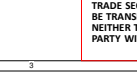
CC80/CC69 close to BV2



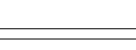
CC1463 close to BR24



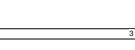
CC1464 close to CP23



CC80/CC69 close to BV2



CC1463 close to BR24



CC1464 close to CP23



CC80/CC69 close to BV2



CC1463 close to BR24



CC1464 close to CP23



CC80/CC69 close to BV2



CC1463 close to BR24



CC1464 close to CP23



CC80/CC69 close to BV2



CC1463 close to BR24



CC1464 close to CP23



CC80/CC69 close to BV2



CC1463 close to BR24



CC1464 close to CP23



CC80/CC69 close to BV2



CC1463 close to BR24



CC1464 close to CP23



CC80/CC69 close to BV2



CC1463 close to BR24



CC1464 close to CP23



CC80/CC69 close to BV2



CC1463 close to BR24



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CC1463 close to BR24



CC1464 close to CP23



CC80/CC69 close to BV2



CC1463 close to BR24



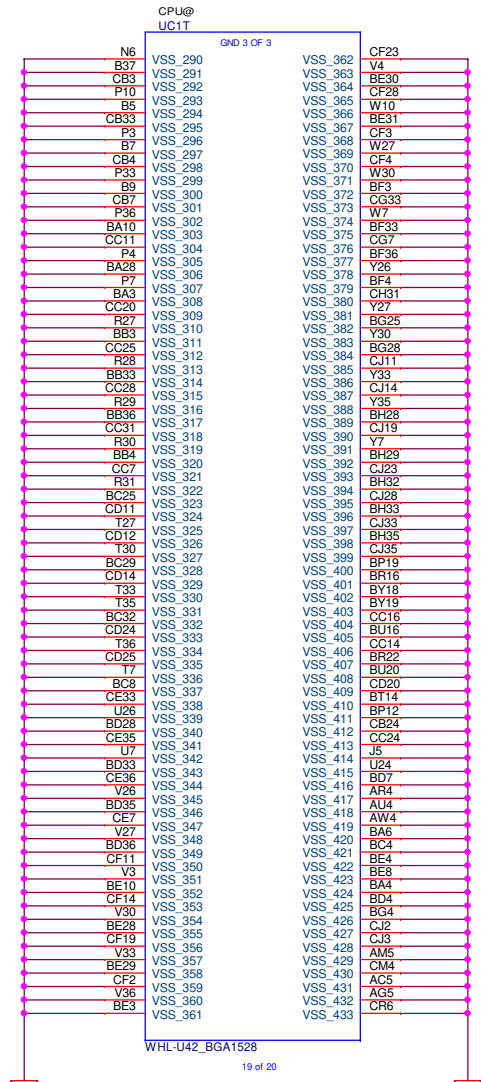
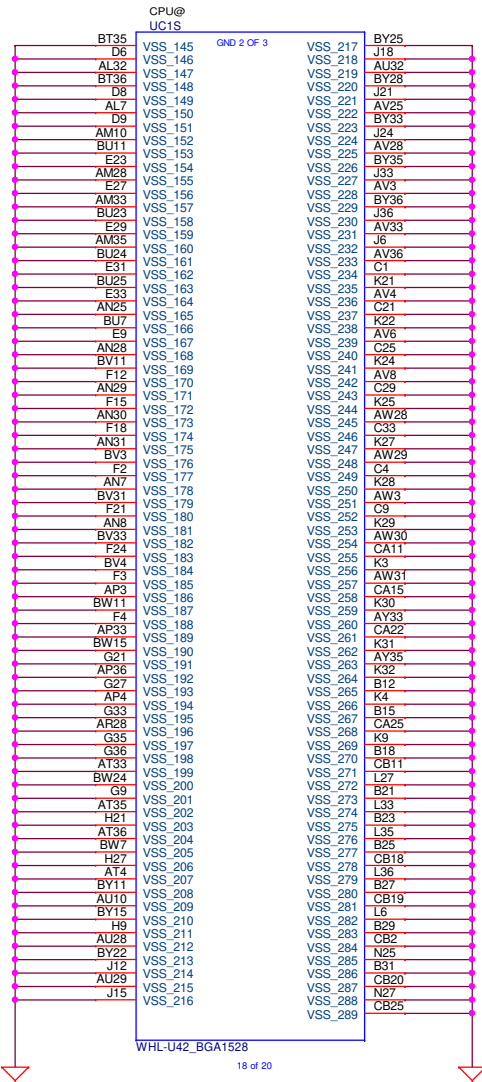
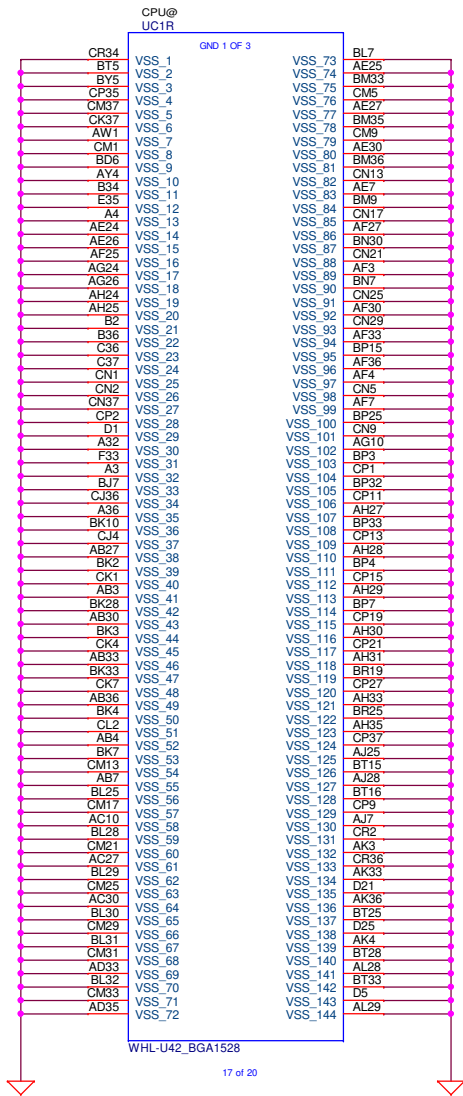
CC1464 close to CP23



CC80/CC69 close to BV2



CC1463 close to BR24



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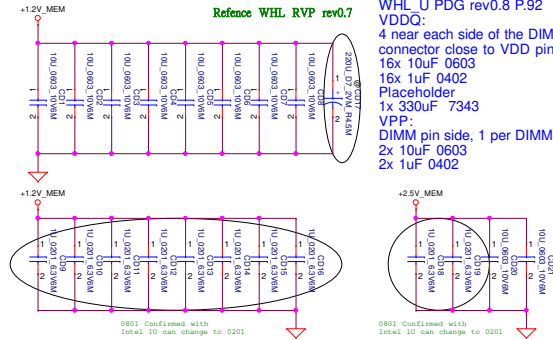


<7> DDR\_A\_DQS[0..7] <<>>  
 <7> DDR\_A\_DQ[0..63] <<>>  
 <7> DDR\_A\_DQS[0..7] <<>>  
 <7> DDR\_A\_MA[0..16] <<>>

Layout Note:  
Place near JDIMM1

Merion Limit height  
CD17 change to SGA0000AM00 H=1.0mm(MAX)

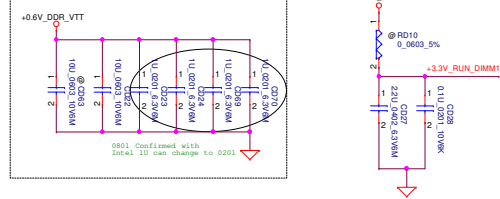
Reference WHL RVP rev0.7



WHL U PDG rev0.8 P.92  
VTT:  
Place on VTT plane close to SODIMM  
2x 10uF 0603(1 cap stuffed, 1 placeholder)  
4x 1uF 0402  
VDDSPD:  
Place close to DIMM  
2x 0.1uF 0402  
2x 2.2uF 0402

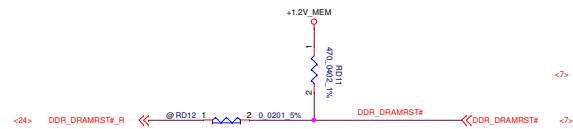
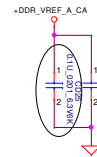
Layout Note:  
Place near JDIMM1.258

Reference WHL RVP rev0.7

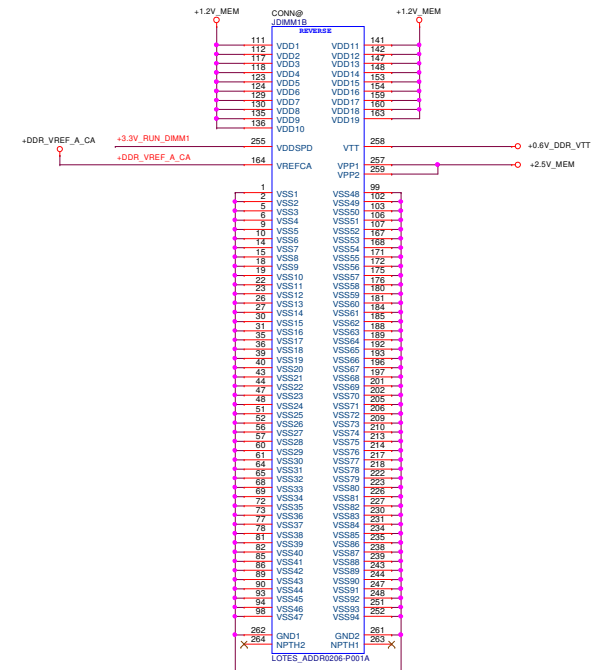
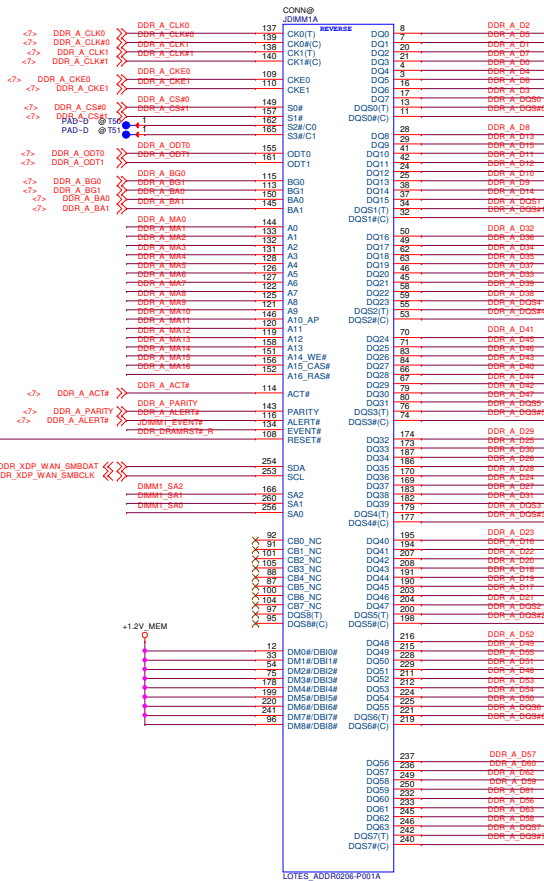


## DIMM Select

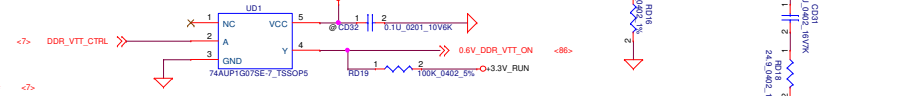
	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0



## Link LOTES\_ADDR0206-P001A02 done 0410



## 6/8 Change to SA00007WE00 DII



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DDR4 DIMMA

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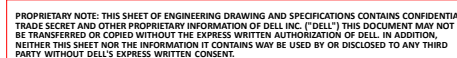
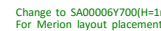
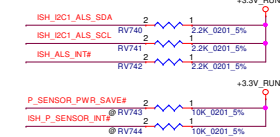
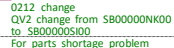
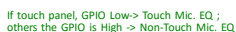
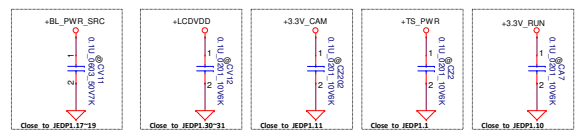
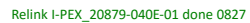
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**Compal Electronics, Inc.**

**DGPU DC/DC Interface**

**LA-G871P**


Title			
Size	Document Number	Rev	
Date: Tuesday, March 05, 2019		Sheet 37 of 109	1.0



Camera Truth table	Mic Only	6mm Normal Camera	6mm IR Camera	3mm IR Camera	2.7mm HD Camera
GPP_G0(CAM_MIC_CBL_DET#)	H	L	L	L	L
GPP_D9(IR_CAM_DET#)	H	H	L	H	H
GPP_C20(3MM_CAM_DET#)	H	H	H	L	H
GPP_A16(2.7MM_CAM_DET#)	H	H	H	H	L
Antenna Location	Bottom	Top	Top	Bottom	Bottom

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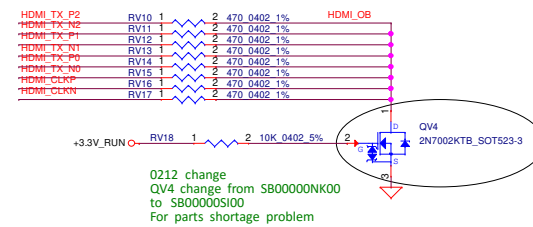
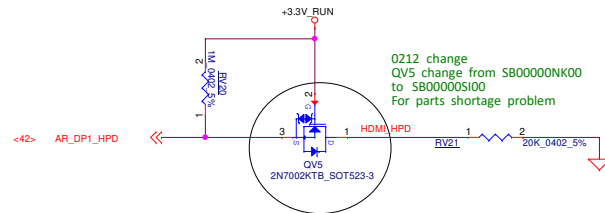
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Title **DP**

Size Document Number **LA-G871P** Rev **1.0**

Date: **Tuesday, March 05, 2019** Sheet **39** of **109**




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Title **CRT**

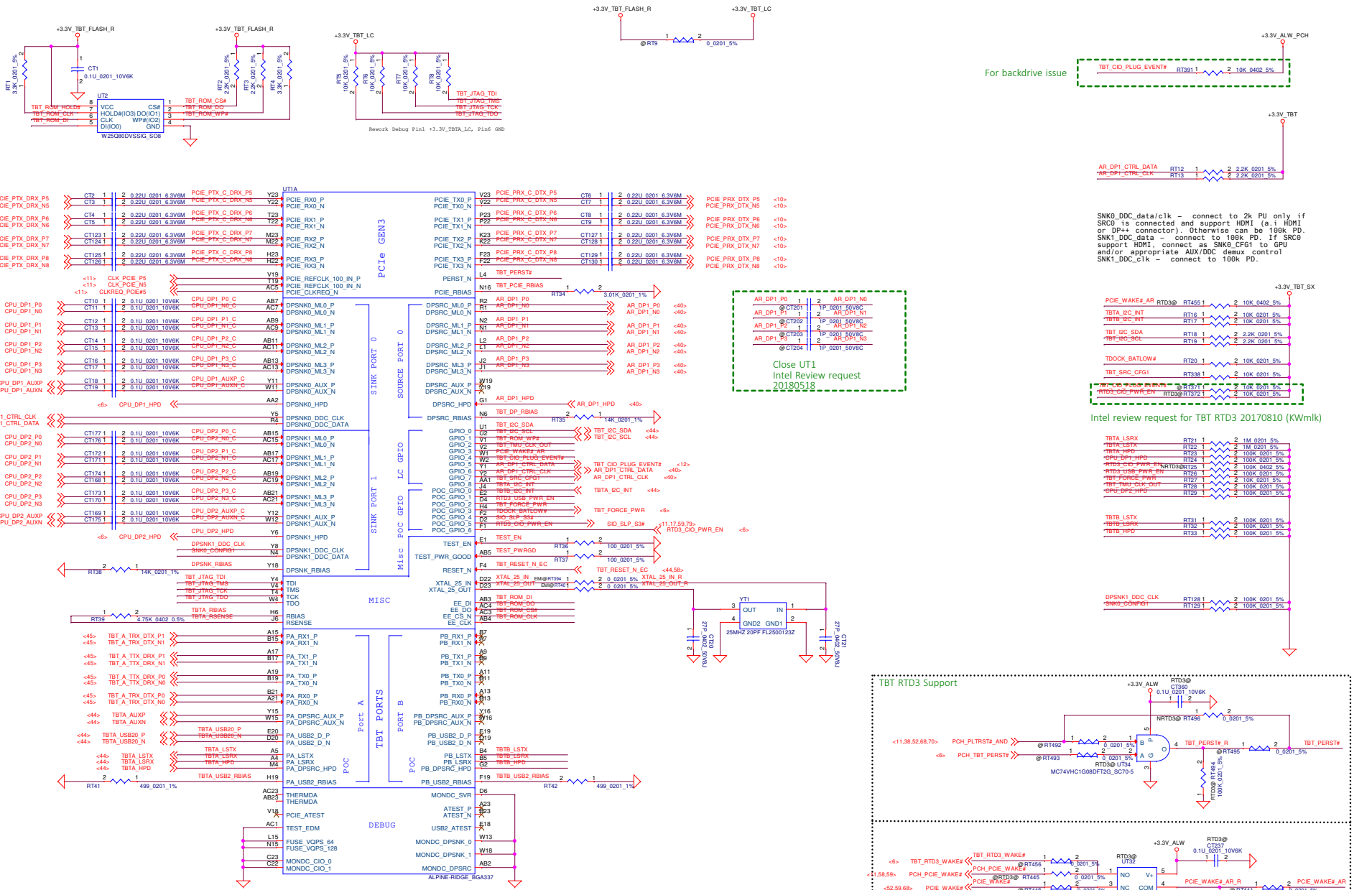
Size	Document Number	Rev
	<b>LA-G871P</b>	<b>1.0</b>

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CPU DD11

CPU DD12

Type C

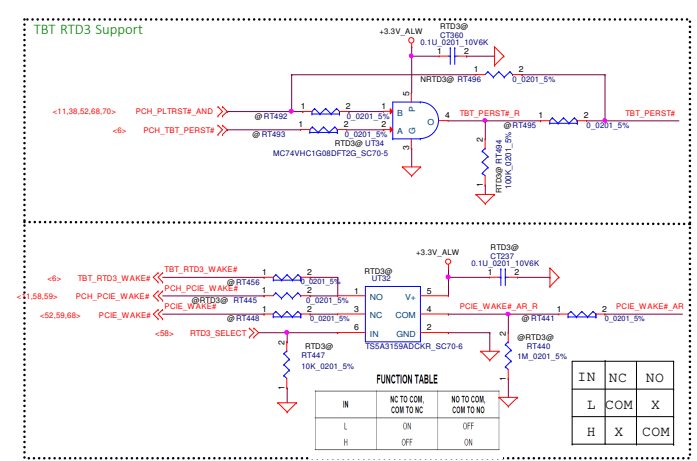


For backdrive issue

SNK0 DDC\_data/clock - connect to 2k PU only if SRC0 is connected and support HDMI (a.i HDMI or DP++ connector). Otherwise can be 100k PD. SNK1 DDC\_data - connect to 100k PD. If TCO support HDMI, connect as SNK0 CF01 to GPU and/or appropriate AUX/DOO demux control SNK1 DDC\_clk - connect to 100k PD.

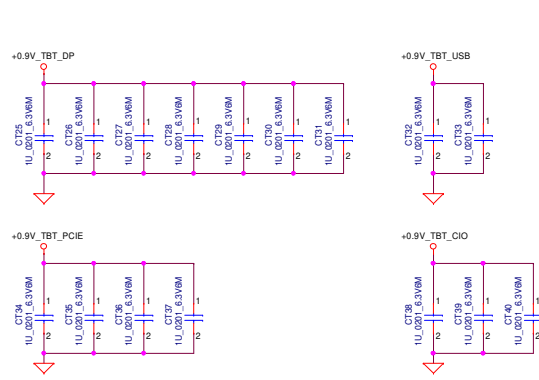
Close UT1  
Intel review request  
20180518

Intel review request for TBT RTD3 20170810 (kWmik)

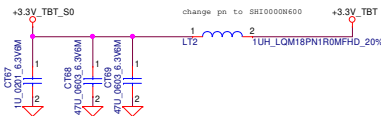


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## TBT Power circuit



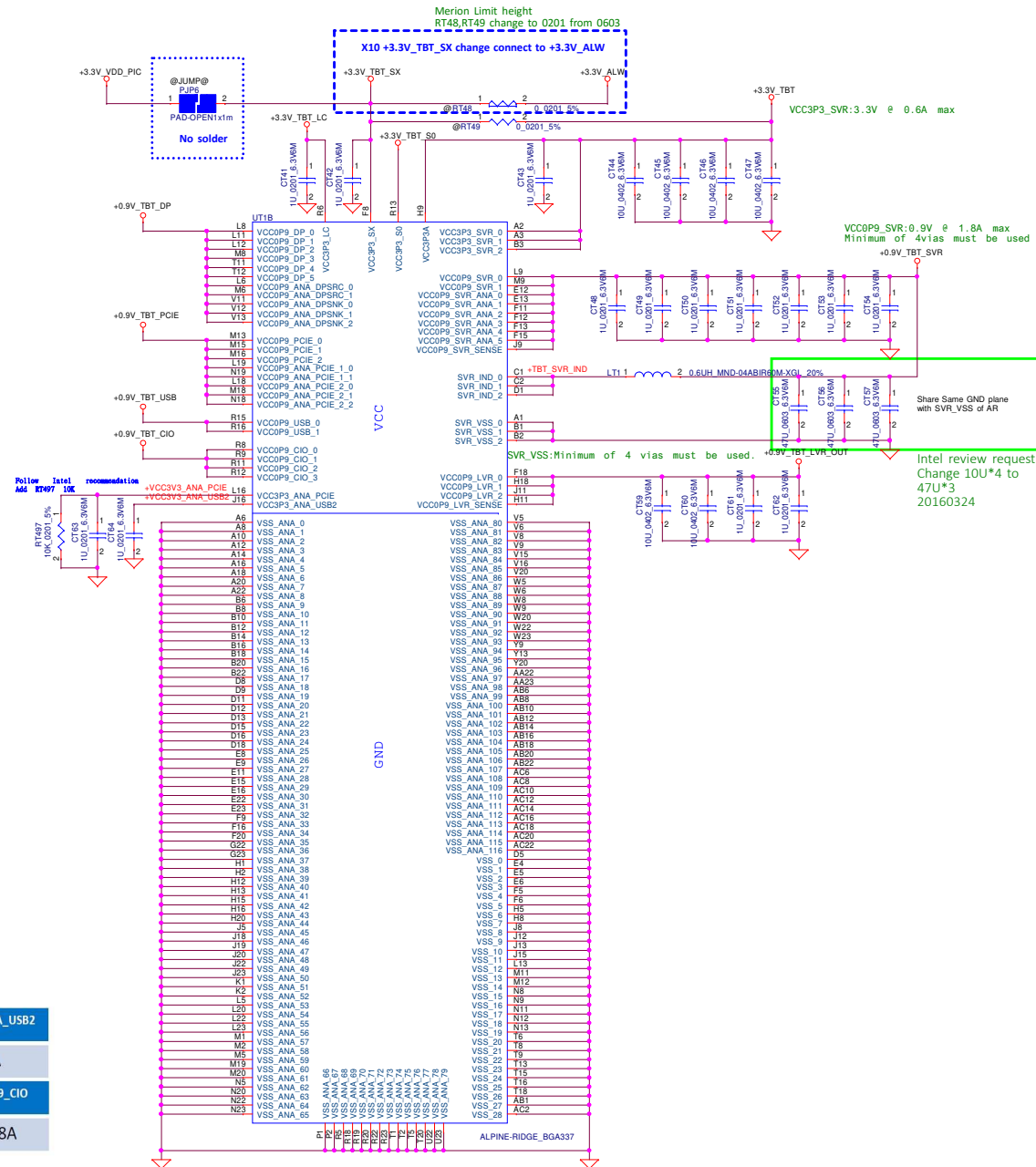
LT2 change footprint to  
CHILI\_PBV160808T-300Y-N\_2P  
follow DFX request



## Power Consumption

- Design power plane supports maximum current requirement

VCC3V3_S0_SYS	VCC3V3_TBT_SX	VCC3V3_IC	VCC3V3_ANA_PCIE	VCC3V3_ANA_USB2	
1.05A	0.19A	0.03A	0.1A	0.1A	
VCC0V9_SVR	VCC0V9_LVR_OUT	VCC0V9_DP	VCC0V9_PCIE	VCC0V9_USB	VCC0V9_CIO
1.83A	0.06A	0.7A	0.58A	0.22A	0.28A



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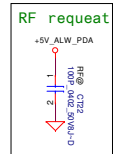
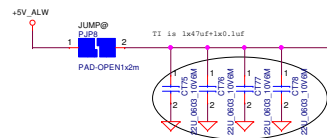
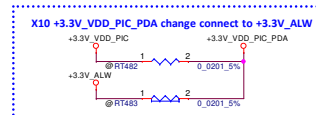
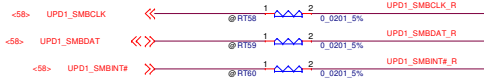
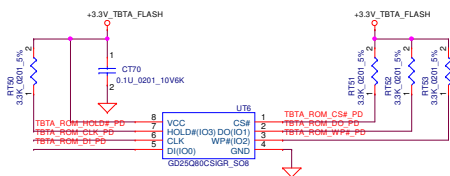
TBT-AR-SP(2/2) VCC/VSS

LA-G871P

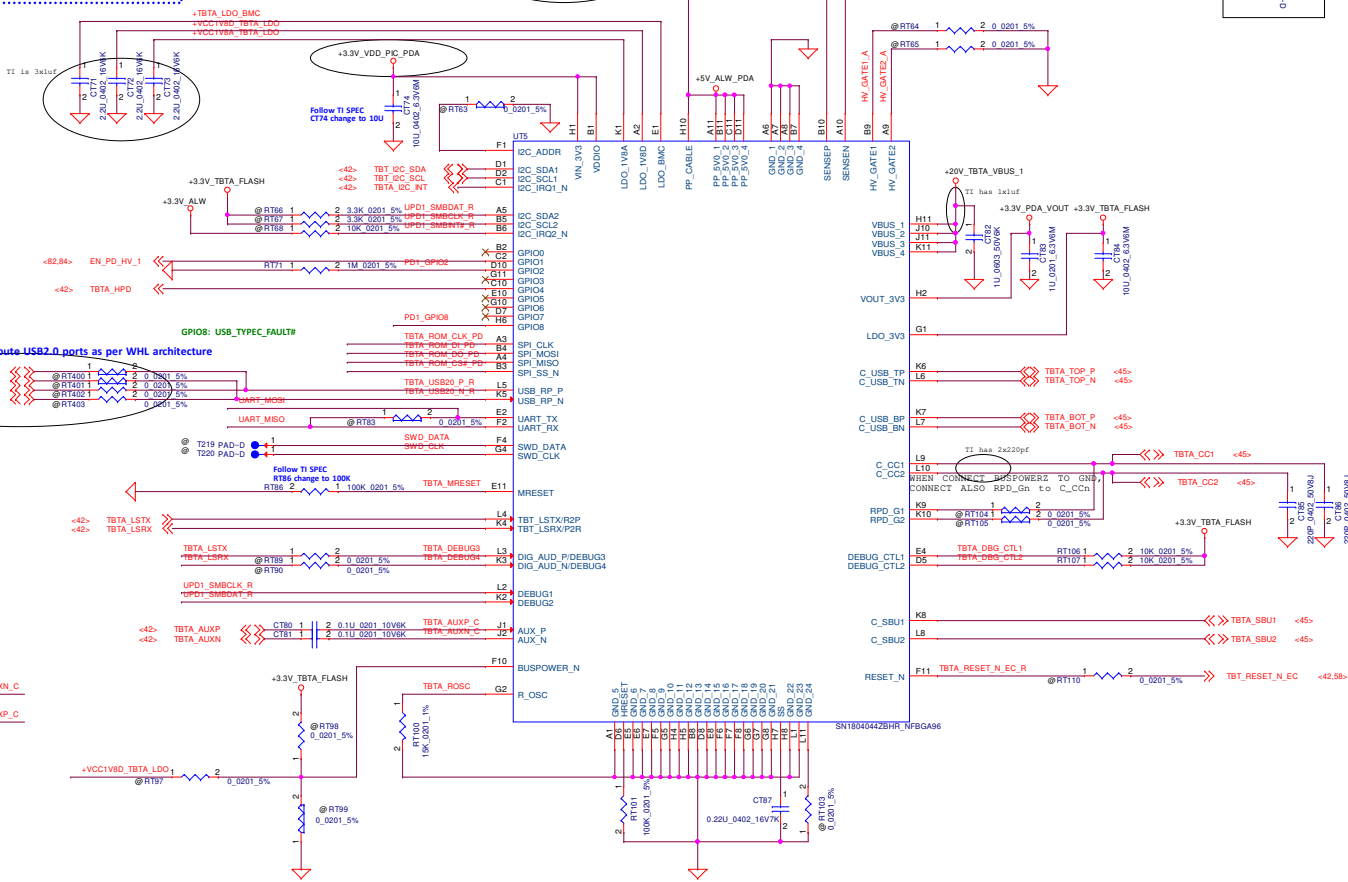
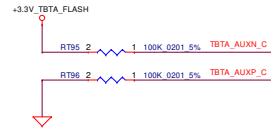
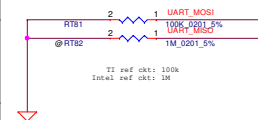
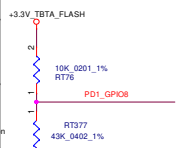
Date: Tuesday, March 05, 2019 Sheet 43 of 109

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For AR port1



DIV = R2/(R1+R2)		Factory	Device	Description
DIV_min	DIV_max	Configuration		
0.00	0.08	0	UFP only 5V @0.9A Sink capability with "Ask for Max" for anything from 0.9-3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported	
0.10	0.18	1	UFP only 5V @0.9A Sink capability with "Ask for Max" for anything from 0.9-3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes -Sink, C and D pin configurations TI VID supported	
0.20	0.28	2	UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported	
0.30	0.38	3	UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes -Sink, C and D pin configurations TI VID supported	
0.40	0.48	4	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported Accepts data and power role swaps, but does not initiate.	
0.50	0.58	5	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations. TI VID supported Accepts power role swaps but will not initiate. Accepts data role swap to UFP and can initiate.	
0.60	0.68	6	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations. TI VID supported Accepts power role swaps but will not initiate. Accepts data role swap to DEP and can initiate.	
0.70	1.00	7	Infinite boot retry from Flash to Host IF cycles.	



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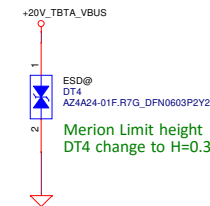
**[Type C]PD Controller T**

Size	Document Number	Rev
	<b>LA-G871P</b>	1.0
Date:	Tuesday, March 05, 2019	Sheet 44 of 109

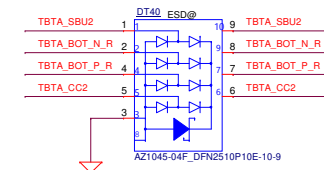
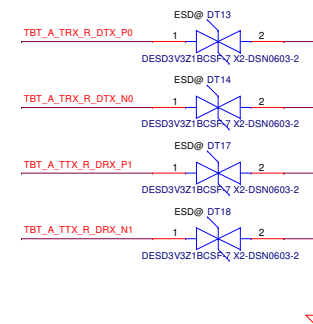
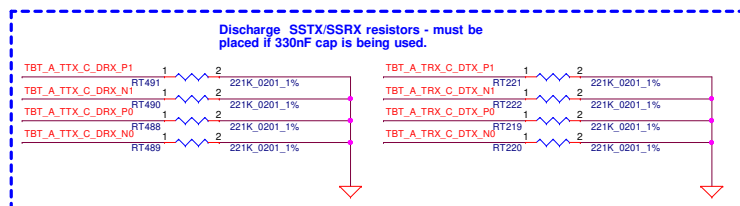
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Merion Limit height  
DT4 change to H=0.32mm(MAX)



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# Reserve

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Title		
TYPE-C Port2 (1/2)		
Size	Document Number	Rev
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Title		
TYPE-C Port2 (2/2)		
Size	Document Number	Rev
	LA-G871P	1.0
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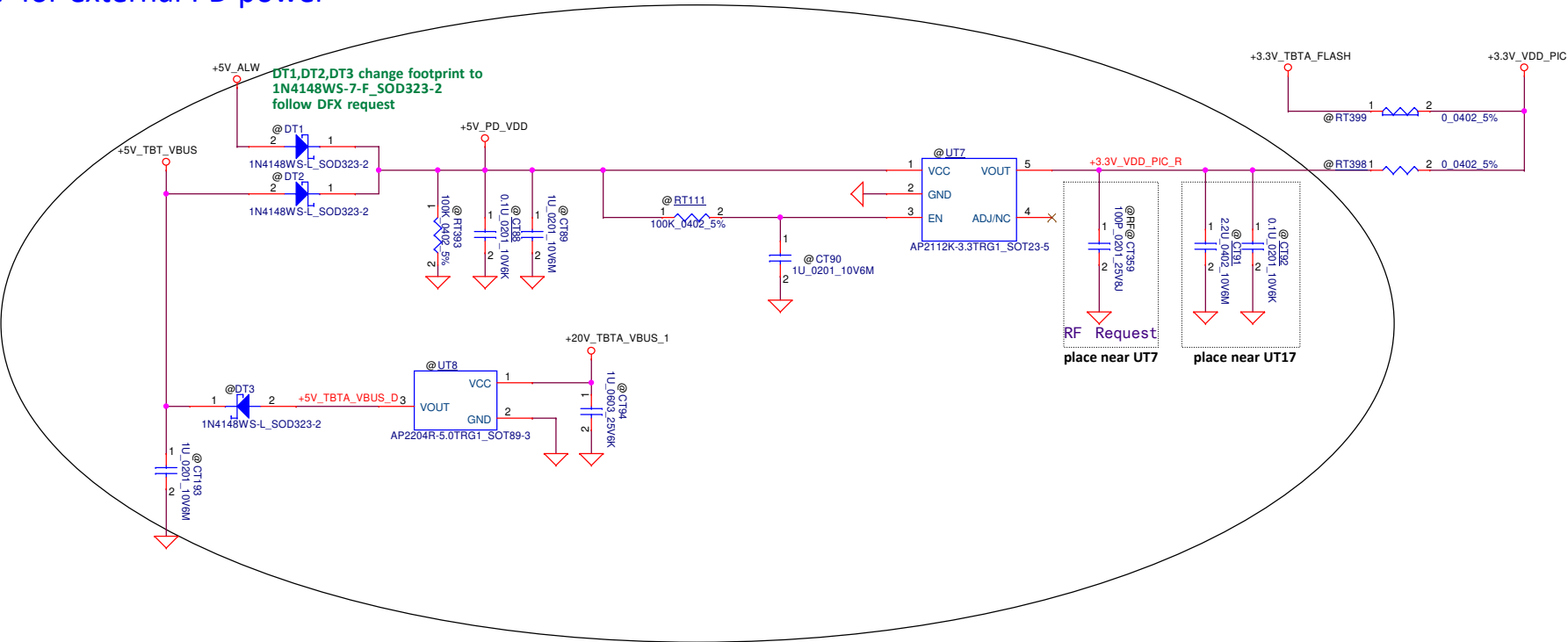
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Title		
TYPE-C Port3 (1/2)		
Size	Document Number	Rev
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Title		
TYPE-C Port3 (2/2)		
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Reserve for external PD power



1031 change

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Title		[Type C]PD Power	
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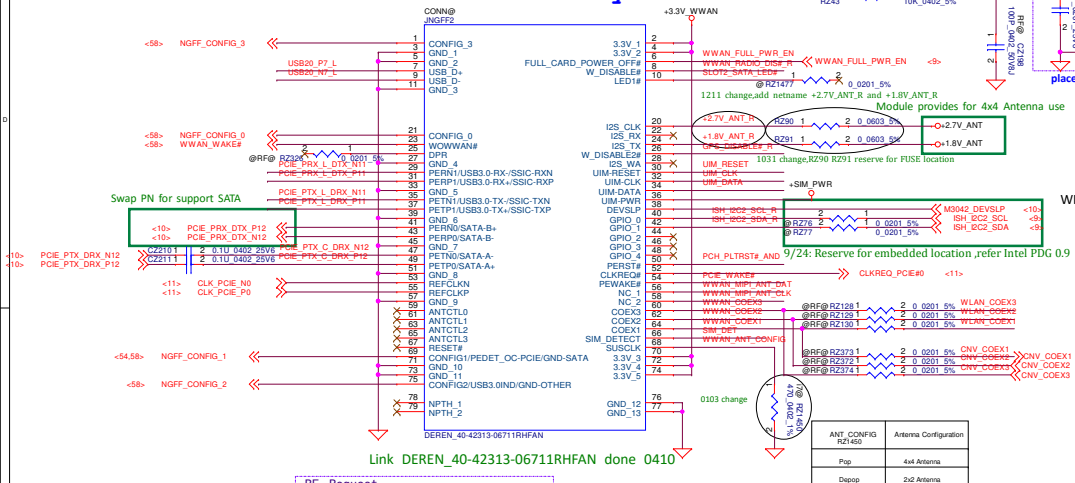
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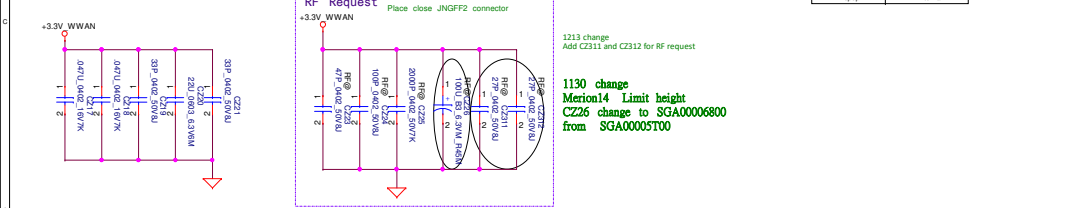
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Compal Electronics, Inc.		
Title		
LAN		
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	LA-G871P	1.0
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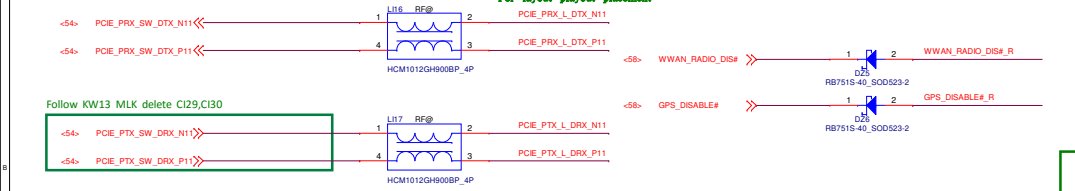
NGFF slot B Key B



Link DEREN\_40-42313-06711RHFAN done 0410

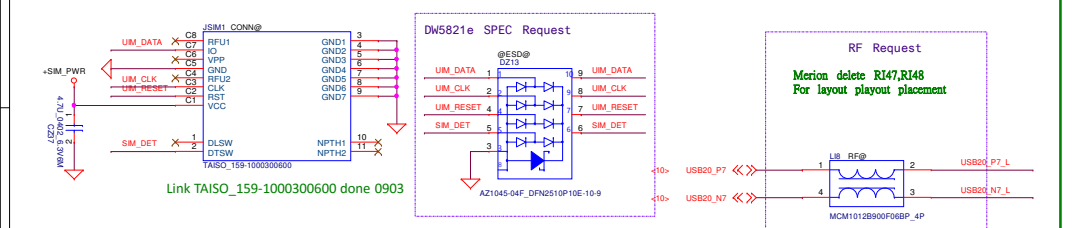


Merion14 swap LI16,LI17 net for layout routing

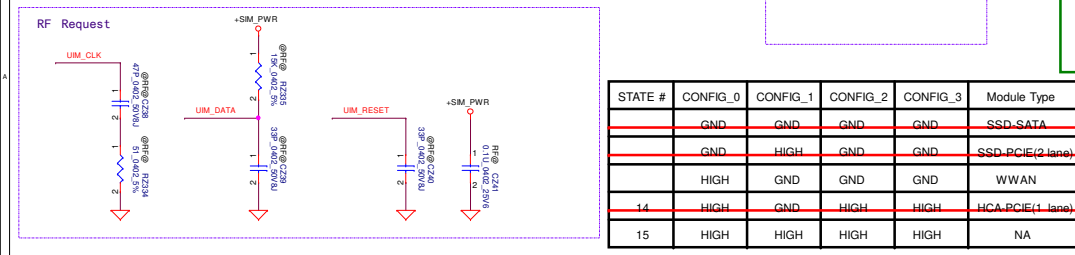


Follow KW13 MLK delete CI29,CI30

## SIM Card Push-Push

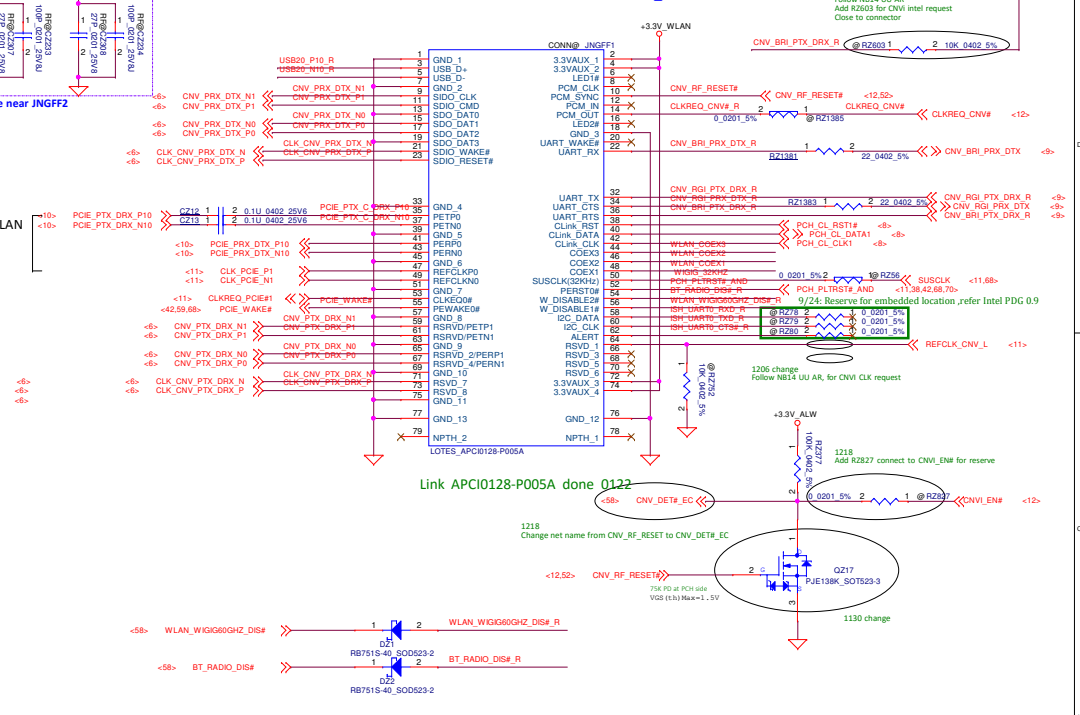


Link TAISO\_159-1000300600 done 0903



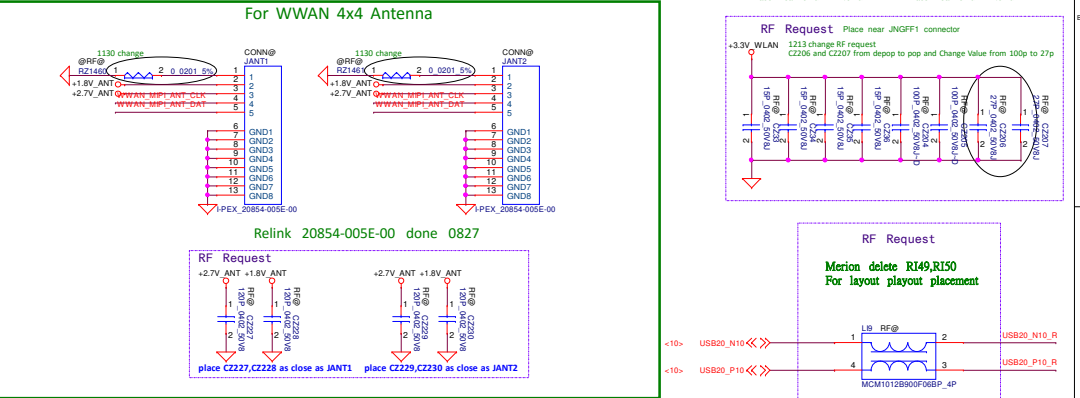
STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type	M3042_PCIE#_SATA
	GND	GND	GND	GND	SSD SATA	High
	GND	HIGH	GND	GND	SSD_PCIE(2 lane)	Low
	HIGH	GND	GND	GND	WWAN	Low
14	HIGH	GND	HIGH	HIGH	HCA_PCIE(1 lane)	Low
15	HIGH	HIGH	HIGH	HIGH	NA	Low

## NGFF slot E Key E



Link APCI0128-P005A done 0122

WWAN\_MIPI\_ANT\_DAT and WWAN\_MIPI\_ANT\_CLK  
(1)The trace length < 30cm  
This max length guidance is practical level of definition  
(2)Spacing to all other signal need 4x line width  
For WWAN 4x4 Antenna



Relink 20854-005E-00 done 0827

1206 change  
Follow NB14 UU AR  
Add RZ603 for CNVi intel request  
Close to connector

777 Add RZ827 connect to CNVI\_EN# for reserve

1130 chance

RF Request Place near JNGFF1 connector

Merion delete RI49,RI50  
For layout playout placement



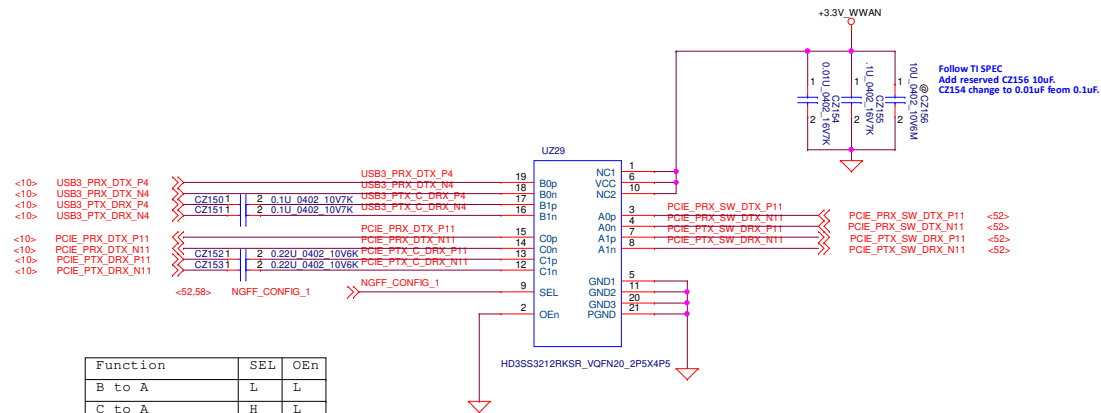
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WIGIG / WIDI		
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# PCIE/USB MUX/DEMUX SW

Link TI HD3SS3212 done



Function	SEL	OEn
B to A	L	L
C to A	H	L
All ports Hi-Z, IC power down	X	H

STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type	M3042_PCIE#_SATA
0	GND	GND	GND	GND	SSD-SATA	HIGH
1	GND	HIGH	GND	GND	SSD-PCIE(2 lane)	LOW
8	HIGH	GND	GND	GND	WWAN	LOW
14	HIGH	GND	HIGH	HIGH	HCA-PCIE(1 lane)	LOW
15	HIGH	HIGH	HIGH	HIGH	NA	LOW

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Compal Electronics, Inc.

USB/PCIE MUX HD3SS3212


LA-G871P

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Title

**Reserve for PCIE device**

Size	Document Number	Rev
	<b>LA-G871P</b>	1.0

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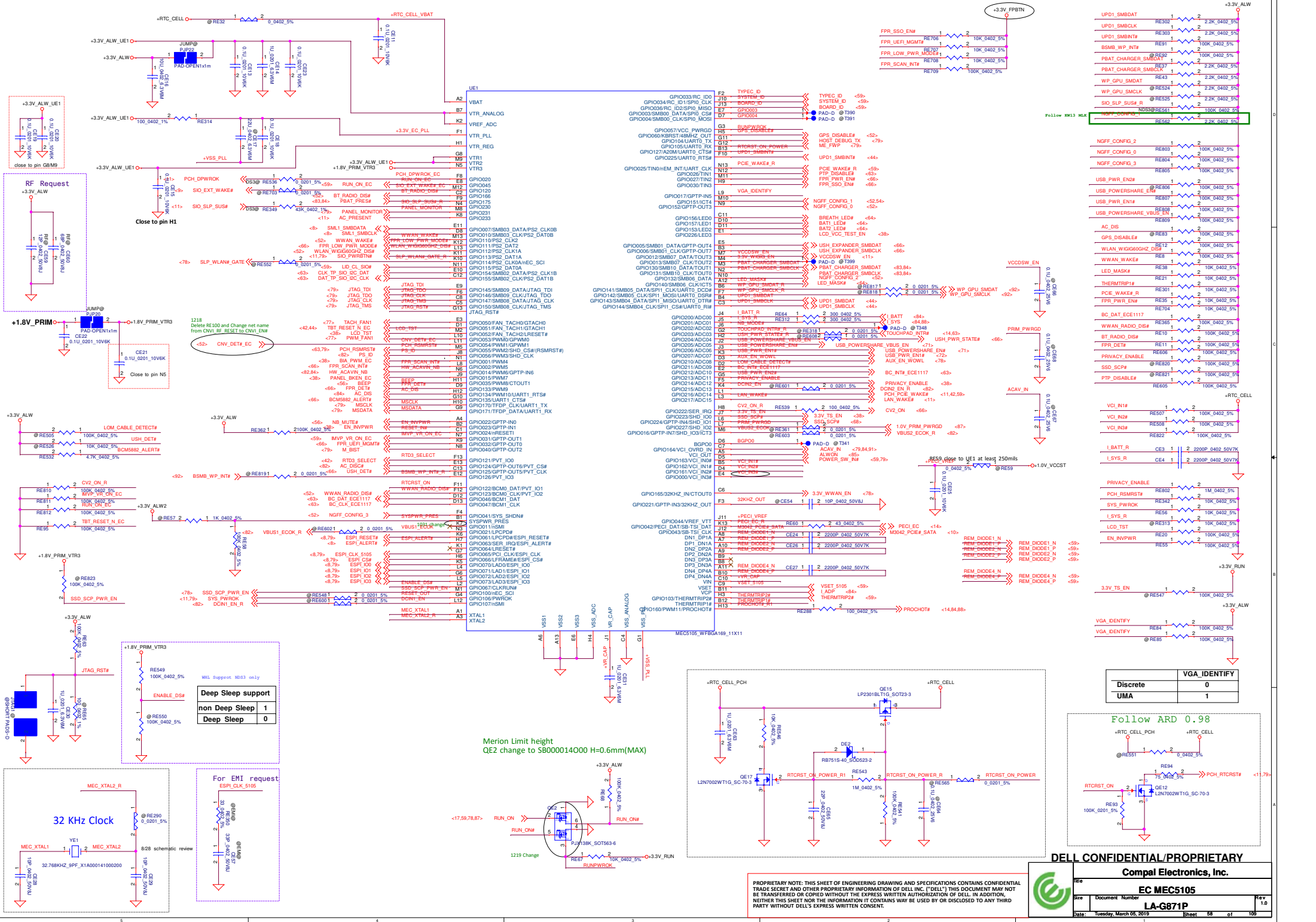
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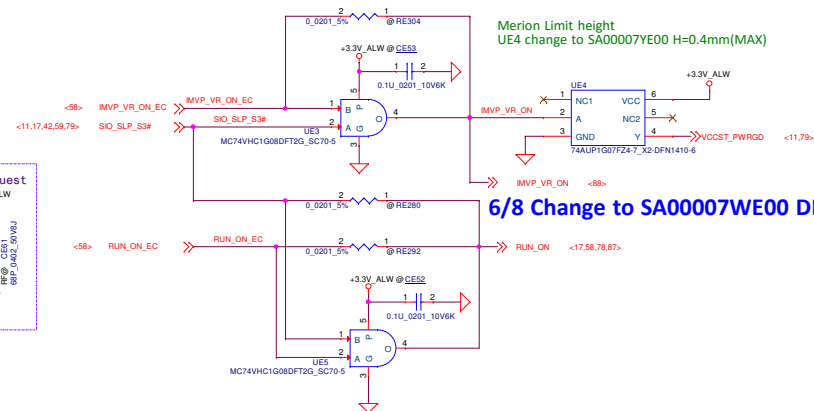
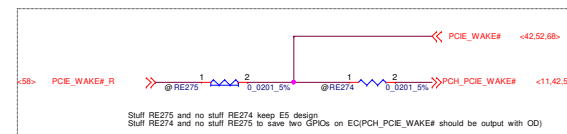
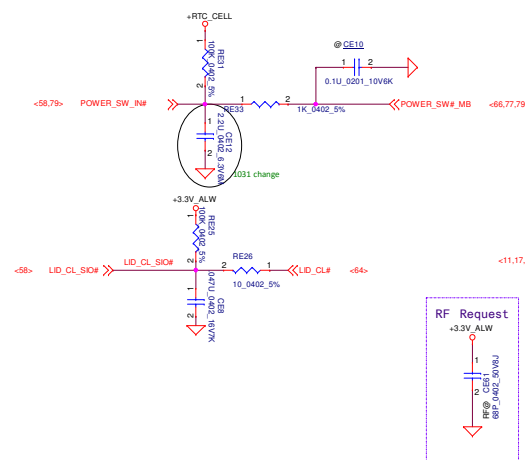


# Reserve

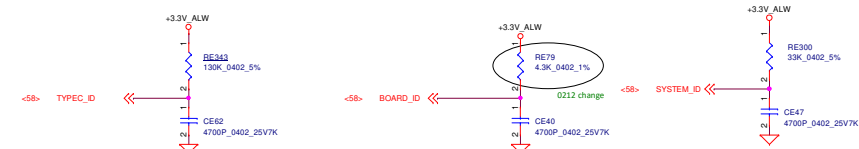
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Compal Electronics, Inc.		
Title		
Audio Ampfilter		
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6/8 Change to SA00007WE00 DII



RE343	CE62	REV
240K	4700p	Single Port ACE w/o AR
* 130K	4700p	Single Port ACE w/AR
62K	4700p	Dual Port ACE w/o AR
33K	4700p	Dual Port ACE w/AR
8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
2K	4700p	.
1K	4700p	.

RE79	CE40	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	reserved
* 4.3K	4700p	A00
2K	4700p	.
1K	4700p	.

RE300	CE47	PANEL SIZE
240K	4700p	11"
130K	4700p	12"
62K	4700p	13"
* 33K	4700p	14"
8.2K	4700p	15"
4.3K	4700p	17"
2K	4700p	15P
1K	4700p	.

TYPEC\_ID rise time is measured from 0%~63.2%.

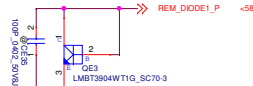
BOARD\_ID rise time is measured from 0%~63.2%.

SYSTEM\_ID rise time is measured from 0%~63.2%.



## Thermal diode mapping

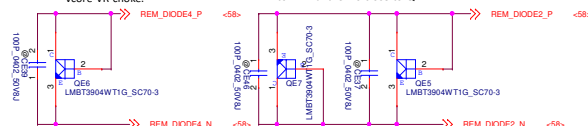
5085 Channel	Locat i on
DP1/DN1	CPU (QE3)
DP2/DN2	2280 SSD (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)

Place under CPU  
Place CE35 close to the QE3 as possible

DP2/DN2 for WiGig on QE5, place QE5 close to WiGig and CE37 close to QE5

DP4/DN4 for Skin on QE6, place QE6 close to Vcore VR choke.

DN2a/DP2a for DDR on QE7, place QE7 close to DDR and CE46 close to QE7



## DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.




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DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title

Secure & Reset IC

Size

Document Number

LA-G871P

Date

Tuesday, March 05, 2019

Sheet

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of

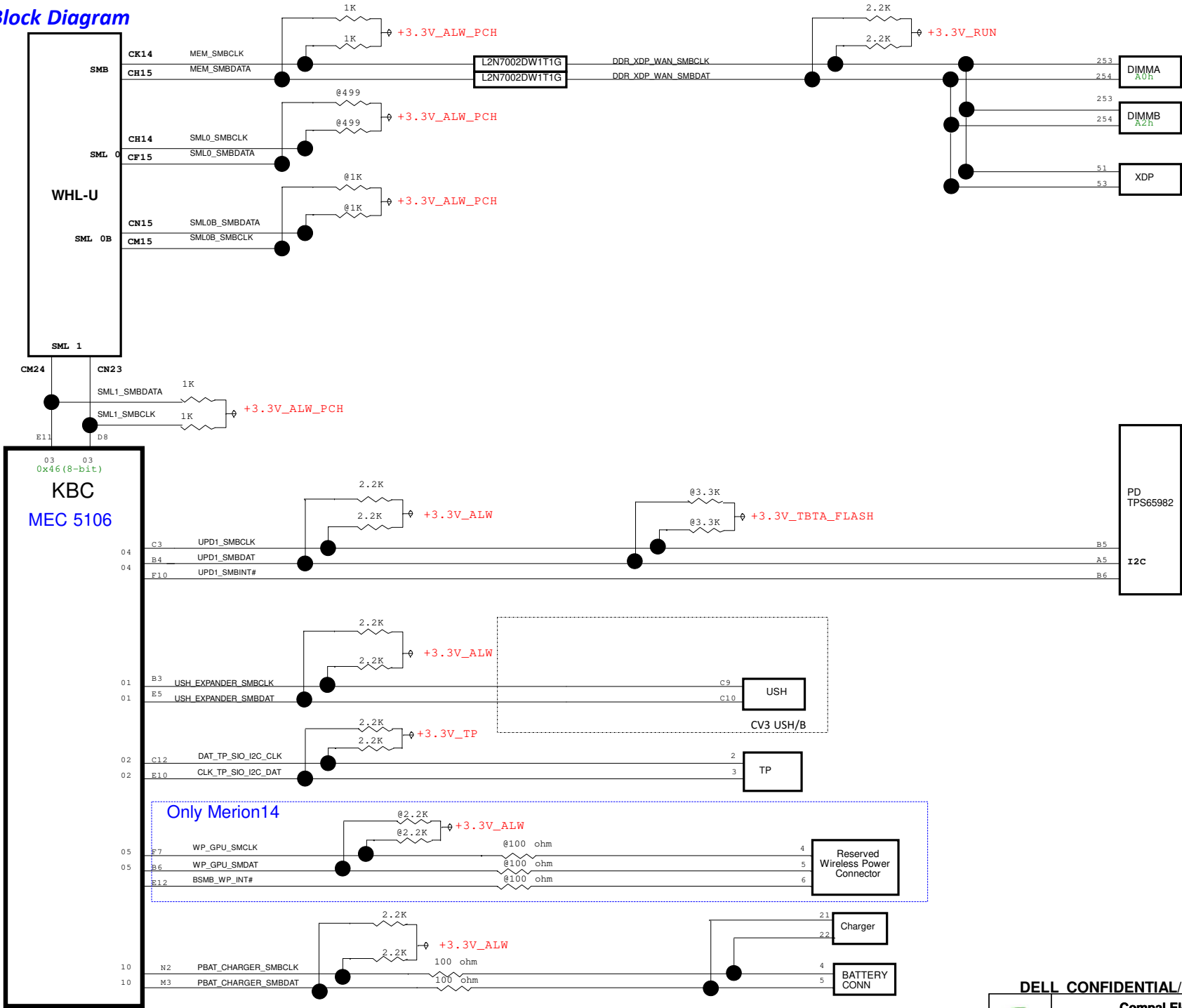
109

Rev

1.0



Merion SMBus Block Diagram



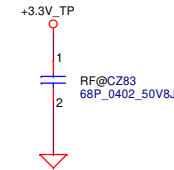
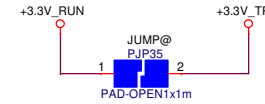
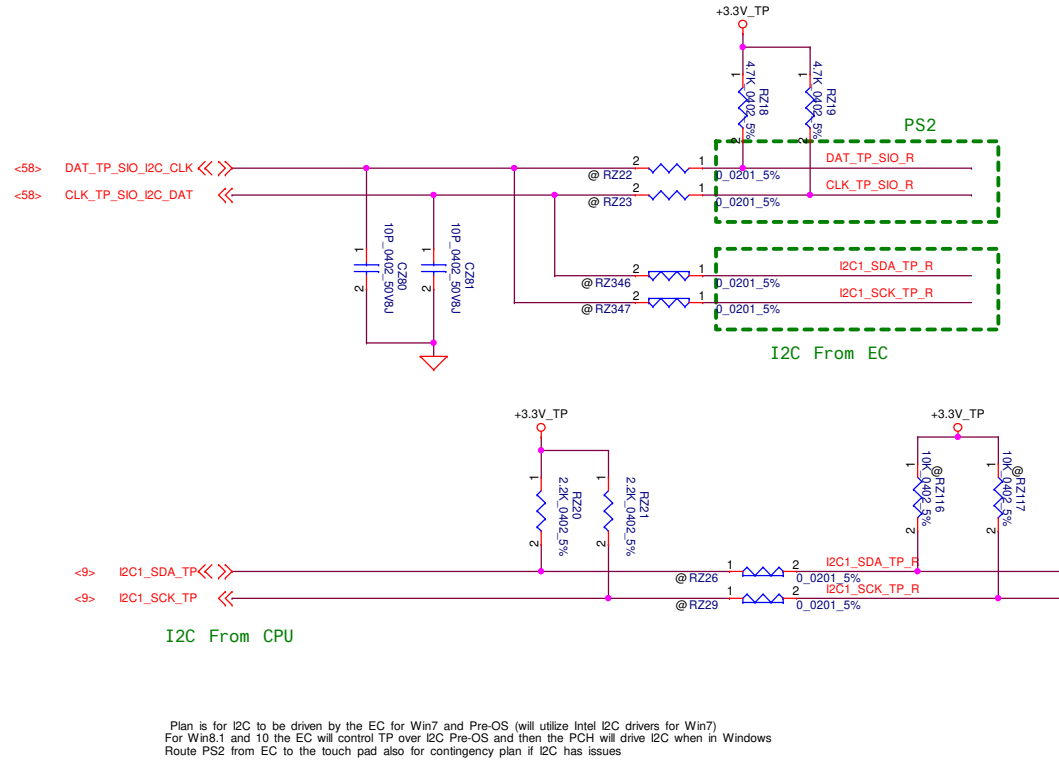
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# Reserve

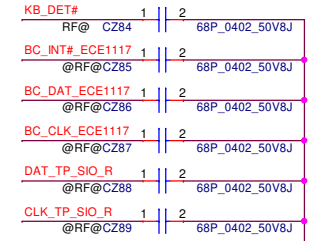
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DELL CONFIDENTIAL/PROPRIETARY		
Compal Electronics, Inc.		
Title		
LEDs (Controller)		
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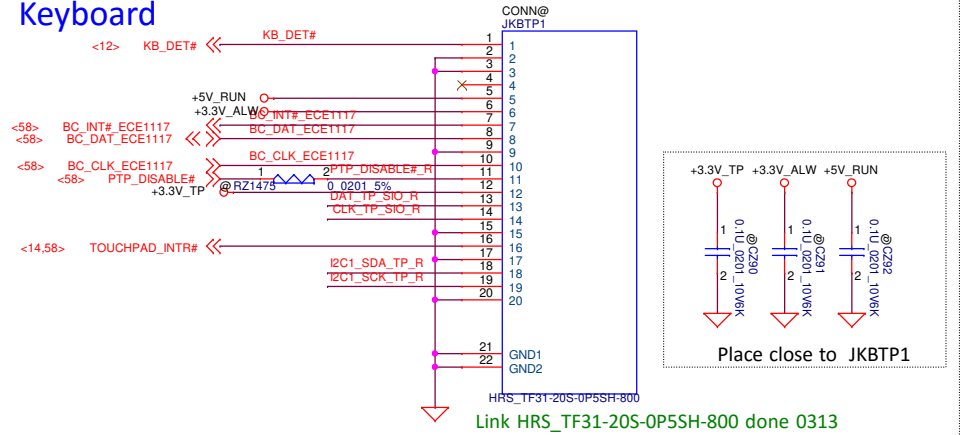
## Touch Pad



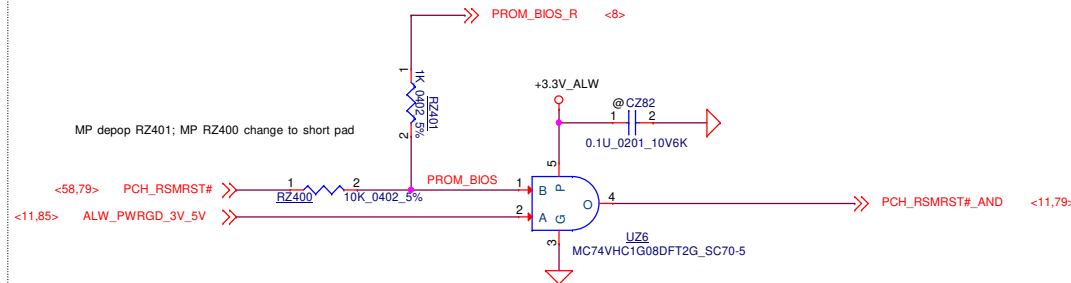
## RF Request



## Keyboard



## RSMRST circuit



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Compal Electronics, Inc.

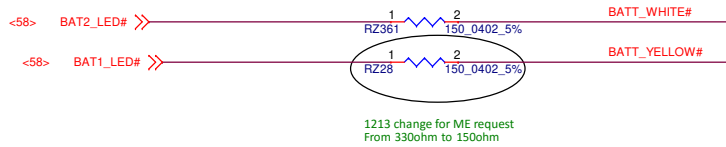
Keyboard

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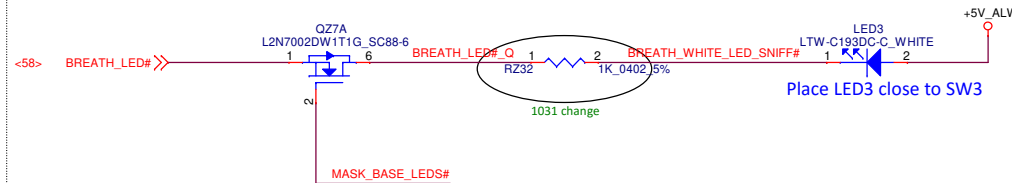
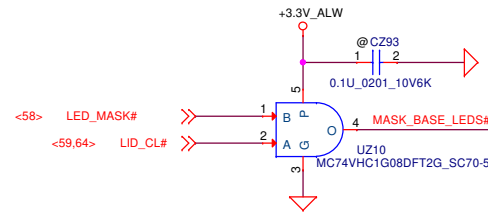
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## Battery LED

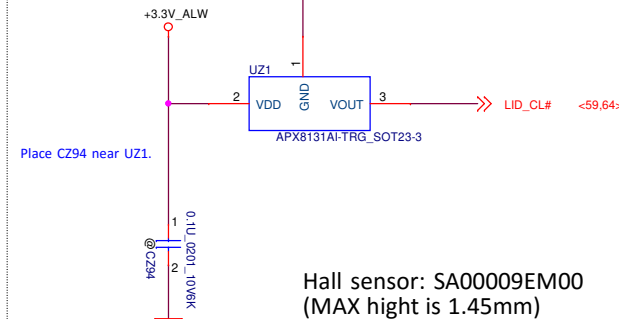


## Breath LED for Merion 14

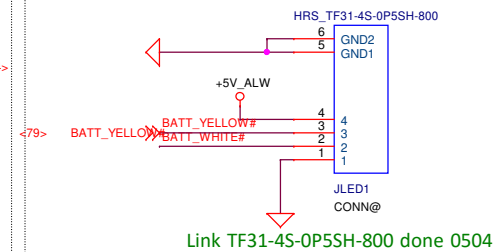
LED P/N change to SC50000FL00 from SC50000BA00



## LID SWITCH



## LED board CONN



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Compal Electronics, Inc.

Title		LED & LID	
Size	Document Number	LA-G871P	
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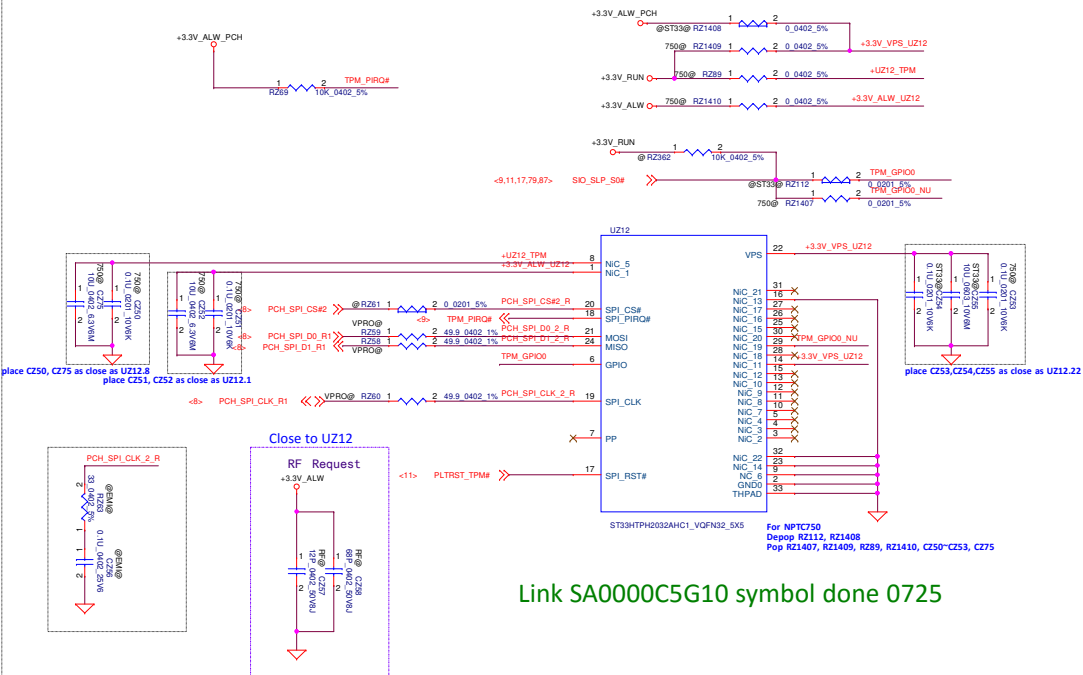
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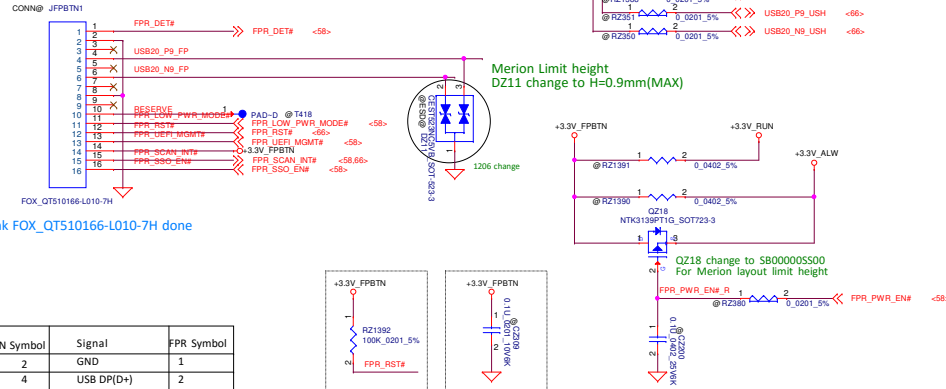
DELL CONFIDENTIAL/PROPRIETARY			
Compal Electronics, Inc.			
Title			
Reserve for KB/TP/LED/LID			
Size	Document Number		Rev
	LA-G871P		1.0
Date:	Tuesday, March 05, 2019		Sheet 65 of 109

# For ST/Nuvoton TPM

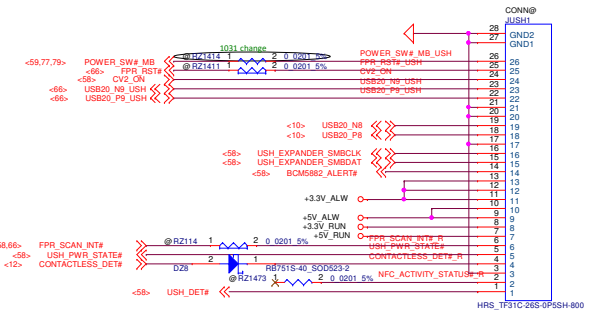
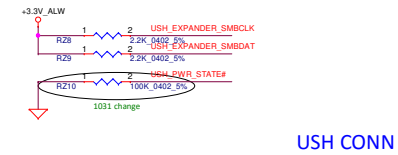
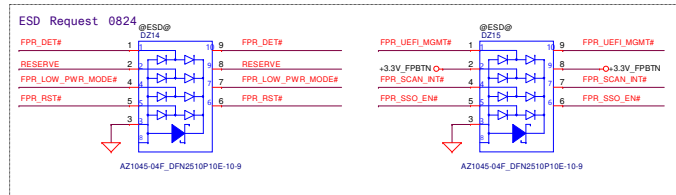


## FP in PWR BUTTON connector

## NEED CONFIRM MODULE PINDEFINE

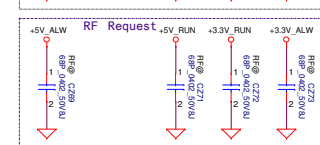
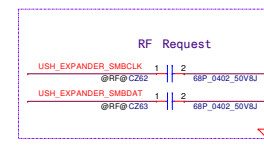
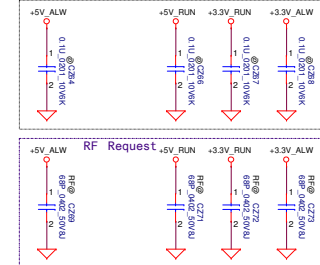


Compal MB CONN Symbol	Signal	FPR Symbol
2	GND	1
4	USB DP(D+)	2
6	USB DM(D-)	3
8	GND	4
10	RESERVED	5
12	FP RESET#	6
14	+3.3V_FPBTN	7
16	FPR_SSO_EN#	8
15	FPR_SCAN_INT#	9
13	FPR_UEFI_MGMT#	10
11	FPR_LOW_PWR_MODE#	11
9	NA	12
7	NA	13
5	NA	14
3	NA	15
1	FPR_DET(GND)	16



Link HRS\_TF31C-26S-0P5SH-800 done 0313

## Close to JUSH1



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Compal Electronics, Inc.



USH & TPM		
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Compal Electronics, Inc.			
Title			
HDD/ODD/FFS Connector			
Size	Document Number		Rev
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Date:	Tuesday, March 05, 2019		Sheet 67 of 109

**Add Power Decoupling for support Intel Teton Glacier**

**RF Request**

Place near JNGFF3

**Place close JNGFF3 pin 12,14,16,18**

**Place close JNGFF3 pin 2,4**

**Place close JNGFF3 pin 70,72,74**

**2280 SSD  
NGFF slot C Key M**

<10> PCIE\_PRX\_DTX\_N13  
<10> PCIE\_PRX\_DTX\_P13

<10> PCIE\_PT\_X\_DRX\_N13  
<10> PCIE\_PT\_X\_DRX\_P13

<10> PCIE\_PRX\_DTX\_N14  
<10> PCIE\_PRX\_DTX\_P14

<10> PCIE\_PT\_X\_DRX\_N14  
<10> PCIE\_PT\_X\_DRX\_P14

<10> PCIE\_PRX\_DTX\_N15  
<10> PCIE\_PRX\_DTX\_P15

<10> PCIE\_PT\_X\_DRX\_N15  
<10> PCIE\_PT\_X\_DRX\_P15

<10> PCIE\_PRX\_DTX\_N16  
<10> PCIE\_PRX\_DTX\_P16

<10> PCIE\_PT\_X\_DRX\_N16  
<10> PCIE\_PT\_X\_DRX\_P16

JNGFF3 CONN@

1	GND_1	3.3VAUX_1	2	N/C_1	2	SUSCLK_R@RN99	1	2	0.0201_5%	<< SUSCLK <11,52>
3	GND_2	3.3VAUX_2	4	N/C_2	3	PEDET (OC-PCle/GND-SATA)	7	3.3VAUX_7		
5	PERn3	N/C_3	6	X	4	GND_12	8	3.3VAUX_8		
7	PERp3	N/C_4	8	X	5	GND_13	9	3.3VAUX_9		
9	GND_3	DAS/DSS#	10	X	6	GND_14	10	X		
11	PETp3	3.3VAUX_3	12	X	7	GND_15	11	X		
13	PETn3	3.3VAUX_4	14	X	8	GND_16	12	X		
15	GND_4	3.3VAUX_5	16	X	9	GND_17	13	X		
17	PERn2	3.3VAUX_6	18	X	10	GND_18	14	X		
19	PERp2	N/C_3	22	X	11	PERn0/SATA-B+	42	X		
21	GND_5	N/C_4	24	X	12	PERp0/SATA-B-	44	X		
23	PETp2	N/C_5	26	X	13	GND_9	46	X		
25	PETn2	N/C_6	28	X	14	PETn0/SATA-A-	48	X		
27	GND_6	N/C_7	30	X	15	PETp0/SATA-A+	50	X		
29	PERn1	N/C_8	32	X	16	REFCLKN	52	X		
31	PERp1	N/C_9	34	X	17	REFCLKP	54	X		
33	GND_7	N/C_10	36	X	18	GND11	56	X		
35	PETn1	N/C_11	38	X	19	NPTH_2	58	X		
37	PETp1	N/C_12	40	X	20	LOTES_APCI0170-P001A				
39	GND_8	N/C_13	42	X						
41	PERn0/SATA-B+	N/C_14	44	X						
43	PERp0/SATA-B-	N/C_15	46	X						
45	GND_9	N/C_16	48	X						
47	PETn0/SATA-A-	N/C_17	50	X						
49	PETp0/SATA-A+	N/C_18	52	X						
51	REFCLKN	DEVSLP	54	X						
53	REFCLKP	N/C_12	40	X						
55	GND11	N/C_13	42	X						
57		N/C_14	44	X						

Key M

Link APCI0170-P001A done 0123

+3.3V\_HDD\_M2 @RN37 1 2 M2280\_DEVSLP 10K\_0402\_5% if signal is PCIE GEN3/SATA GEN3 maybe change C value or no need for DG0.9 SATA EXPRESS HDD

M2280\_PCIE\_SATL# <10>

SSD\_SCPL\_R@RN1291 NVME\_LED# @RN100 0.0201\_5% << SSD\_SCPL# <58>

SSD\_SCLK\_R@RN99 1 2 0.0201\_5% << SUSCLK <11,52>

PCIE\_WAKE# PCH\_PLTRST#\_AND CLKREQ\_PCIE#2 <11,38,42,52,70> <11> << PCIE\_WAKE# <42,52,59>

+3.3V\_SSD from SSD storage protection power gate control  
0212 change  
RN130 covering green printing for co-lay materials

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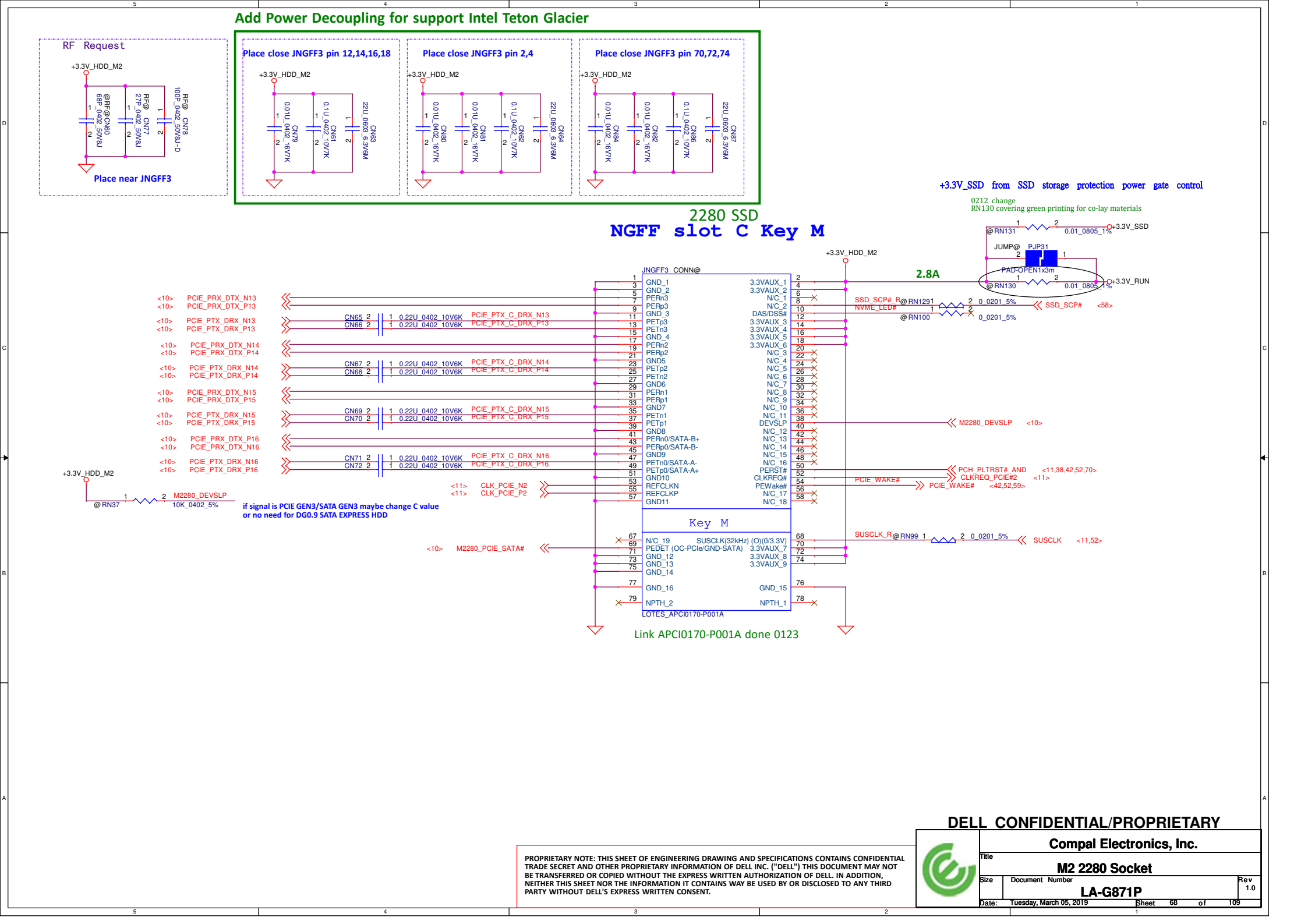
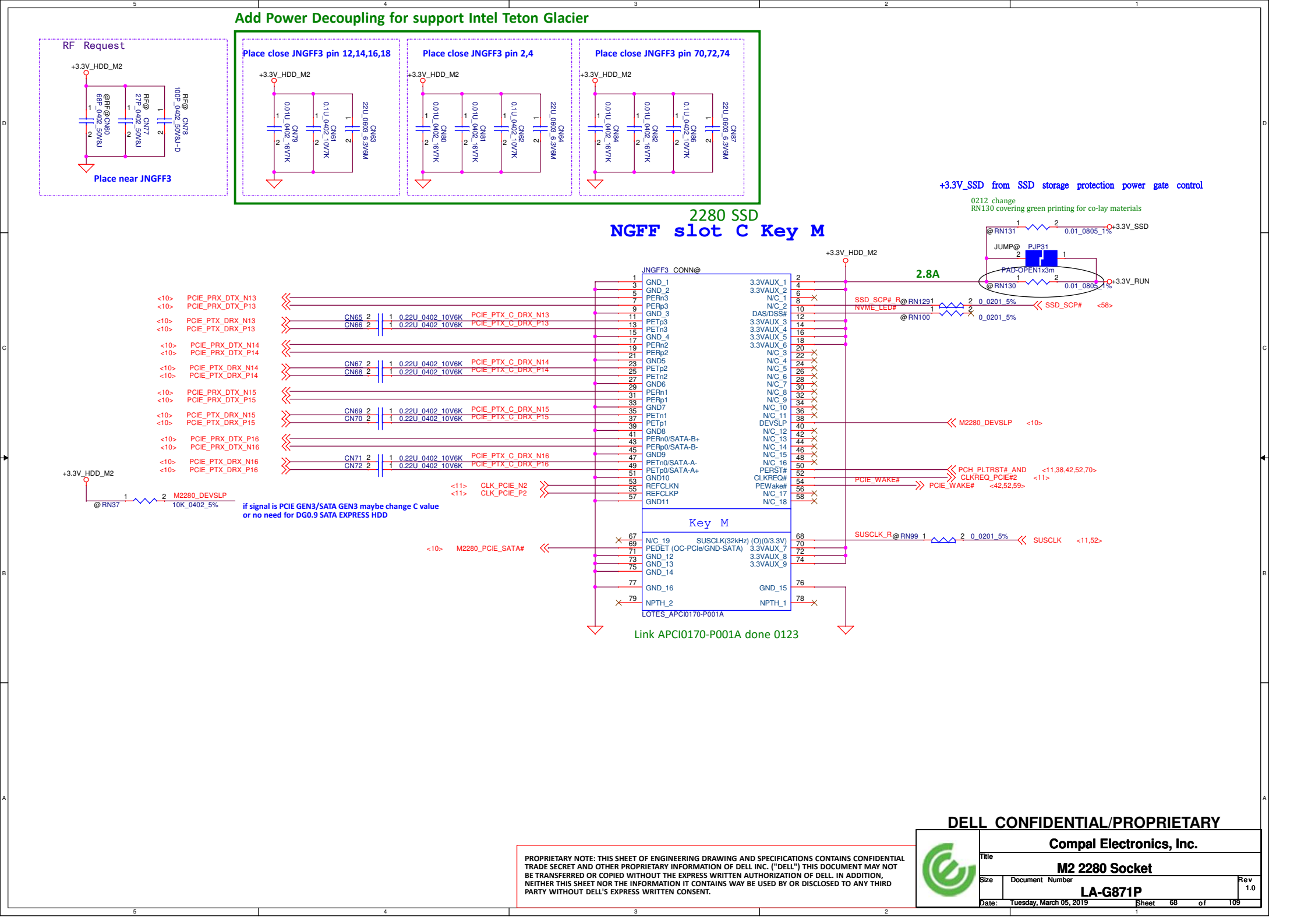
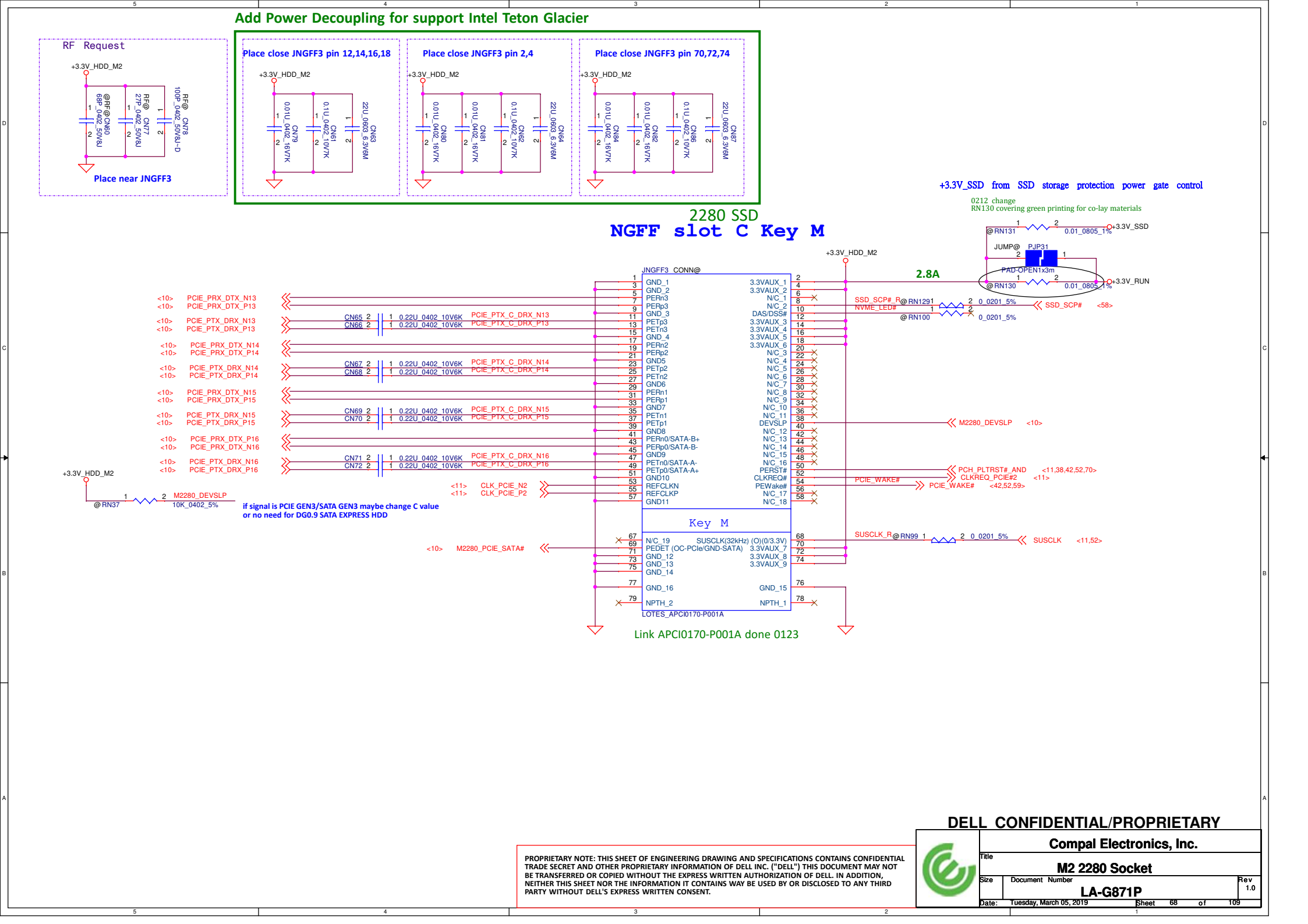
**Compal Electronics, Inc.**

Title: **M2 2280 Socket**

Size: Document Number **LA-G871P** Rev 1.0

Date: Tuesday, March 05, 2019 Sheet 68 of 109

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[illegible]

RF Request

Place near JNGFF3

Place close JNGFF3 pin 12,14,16,18

Place close JNGFF3 pin 2,4

Place close JNGFF3 pin 70,72,74

2280 SSD  
NGFF slot C Key M

3.3V\_HDD\_M2

3.3V\_SSD from SSD storage protection power gate control

0212 change  
RN130 covering green printing for co-lay materials

JNGFF3 CONN@

3.3V\_AUX\_1

3.3V\_AUX\_2

3.3V\_AUX\_3

3.3V\_AUX\_4

3.3V\_AUX\_5

3.3V\_AUX\_6

3.3V\_AUX\_7

3.3V\_AUX\_8

3.3V\_AUX\_9

3.3V\_AUX\_10

3.3V\_AUX\_11

3.3V\_AUX\_12

3.3V\_AUX\_13

3.3V\_AUX\_14

3.3V\_AUX\_15

3.3V\_AUX\_16

3.3V\_AUX\_17

3.3V\_AUX\_18

3.3V\_AUX\_19

3.3V\_AUX\_20

3.3V\_AUX\_21

3.3V\_AUX\_22

3.3V\_AUX\_23

3.3V\_AUX\_24

3.3V\_AUX\_25

3.3V\_AUX\_26

3.3V\_AUX\_27

3.3V\_AUX\_28

3.3V\_AUX\_29

3.3V\_AUX\_30

3.3V\_AUX\_31

3.3V\_AUX\_32

3.3V\_AUX\_33

3.3V\_AUX\_34

3.3V\_AUX\_35

3.3V\_AUX\_36

3.3V\_AUX\_37

3.3V\_AUX\_38

3.3V\_AUX\_39

3.3V\_AUX\_40

3.3V\_AUX\_41

3.3V\_AUX\_42

3.3V\_AUX\_43

3.3V\_AUX\_44

3.3V\_AUX\_45

3.3V\_AUX\_46

3.3V\_AUX\_47

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3.3V\_AUX\_60

3.3V\_AUX\_61

3.3V\_AUX\_62

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3.3V\_AUX\_66

3.3V\_AUX\_67

3.3V\_AUX\_68

3.3V\_AUX\_69

3.3V\_AUX\_70

3.3V\_AUX\_71

3.3V\_AUX\_72

3.3V\_AUX\_73

3.3V\_AUX\_74

3.3V\_AUX\_75

3.3V\_AUX\_76

3.3V\_AUX\_77

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3.3V\_AUX\_79

3.3V\_AUX\_80

3.3V\_AUX\_81

3.3V\_AUX\_82

3.3V\_AUX\_83

3.3V\_AUX\_84

3.3V\_AUX\_85

3.3V\_AUX\_86

3.3V\_AUX\_87

3.3V\_AUX\_88

3.3V\_AUX\_89

3.3V\_AUX\_90

3.3V\_AUX\_91

3.3V\_AUX\_92

3.3V\_AUX\_93

3.3V\_AUX\_94

3.3V\_AUX\_95

3.3V\_AUX\_96

3.3V\_AUX\_97

3.3V\_AUX\_98

3.3V\_AUX\_99

3.3V\_AUX\_100

3.3V\_AUX\_101

3.3V\_AUX\_102

3.3V\_AUX\_103

3.3V\_AUX\_104

3.3V\_AUX\_105

3.3V\_AUX\_106

3.3V\_AUX\_107

3.3V\_AUX\_108

3.3V\_AUX\_109

3.3V\_AUX\_110

3.3V\_AUX\_111

3.3V\_AUX\_112

3.3V\_AUX\_113

3.3V\_AUX\_114

3.3V\_AUX\_115

3.3V\_AUX\_116

3.3V\_AUX\_117

3.3V\_AUX\_118

3.3V\_AUX\_119

3.3V\_AUX\_120

3.3V\_AUX\_121

3.3V\_AUX\_122

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3.3V\_AUX\_287

RF Request

Place near JNGFF3

Place close JNGFF3 pin 12,14,16,18

Place close JNGFF3 pin 2,4

Place close JNGFF3 pin 70,72,74

2280 SSD  
NGFF slot C Key M

3.3V\_HDD\_M2

3.3V\_SSD from SSD storage protection power gate control

0212 change  
RN130 covering green printing for co-lay materials

JNGFF3 CONN@

3.3V\_AUX\_1

3.3V\_AUX\_2

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3.3V\_AUX\_286

3.3V\_AUX\_287

**Add Power Decoupling for support Intel Teton Glacier**

**RF Request**

Place near JNGFF3

**Place close JNGFF3 pin 12,14,16,18**

**Place close JNGFF3 pin 2,4**

**Place close JNGFF3 pin 70,72,74**

**2280 SSD  
NGFF slot C Key M**

<10> PCIE\_PRX\_DTX\_N13  
<10> PCIE\_PRX\_DTX\_P13

<10> PCIE\_PT\_X\_DRX\_N13  
<10> PCIE\_PT\_X\_DRX\_P13

<10> PCIE\_PRX\_DTX\_N14  
<10> PCIE\_PRX\_DTX\_P14

<10> PCIE\_PT\_X\_DRX\_N14  
<10> PCIE\_PT\_X\_DRX\_P14

<10> PCIE\_PRX\_DTX\_N15  
<10> PCIE\_PRX\_DTX\_P15

<10> PCIE\_PT\_X\_DRX\_N15  
<10> PCIE\_PT\_X\_DRX\_P15

<10> PCIE\_PRX\_DTX\_N16  
<10> PCIE\_PRX\_DTX\_P16

<10> PCIE\_PT\_X\_DRX\_N16  
<10> PCIE\_PT\_X\_DRX\_P16

JNGFF3 CONN@

Pin	Signal	Component
1	GND_1	
3	3.3VAUX_1	
5	GND_2	
7	PERn3	
9	PERp3	
11	GND_3	
13	PETp3	
15	PETn3	
17	GND_4	
19	PERn2	
21	PERp2	
23	GND_5	
25	PETp2	
27	PETn2	
29	GND_6	
31	PERn1	
33	PERp1	
35	GND_7	
37	PETn1	
39	PETp1	
41	GND_8	
43	PERn0/SATA-B+	
45	PERp0/SATA-B-	
47	GND_9	
49	PETn0/SATA-A-	
51	PETp0/SATA-A+	
53	REFCLKN	
55	REFCLKP	
57	GND11	

**Key M**

Pin	Signal	Component
67	N/C_19	SUSCLK(32kHz) (O)(I)/0.3.3V
69	PEDET (OC-PCle/GND-SATA)	3.3VAUX_7
71	GND_12	3.3VAUX_8
73	GND_13	3.3VAUX_9
75	GND_14	
77	GND_16	
79	NPTH_2	NPTH_1

Link APCI0170-P001A done 0123

+3.3V\_HDD\_M2

M2280\_DEVSLP <10>

if signal is PCIE GEN3/SATA GEN3 maybe change C value or no need for DG0.9 SATA EXPRESS HDD

SSD\_SCP#\_R @RN1291 0 0.0201\_5% << SSD\_SCP# <58>

NVME\_LED# @RN100 0 0.0201\_5%

PCIE\_WAKE# <> PCH\_PLTRST#\_AND CLKREQ\_PCIE#2 <11,38,42,52,70> <11>

PCIE\_WAKE# <> PCIE\_WAKE# <42,52,59>

SUSCLK\_R @RN99 1 0 0.0201\_5% << SUSCLK <11,52>

+3.3V\_SSD from SSD storage protection power gate control

0212 change RN130 covering green printing for co-lay materials

**DELL CONFIDENTIAL/PROPRIETARY**

**Compal Electronics, Inc.**

Title: **M2 2280 Socket**

Size: Document Number **LA-G871P** Rev 1.0

Date: Tuesday, March 05, 2019 Sheet 68 of 109

**Add Power Decoupling for support Intel Teton Glacier**

**RF Request**

+3.3V\_HDD\_M2

Place near JNGFF3

**Place close JNGFF3 pin 12,14,16,18**

+3.3V\_HDD\_M2

**Place close JNGFF3 pin 2,4**

+3.3V\_HDD\_M2

**Place close JNGFF3 pin 70,72,74**

+3.3V\_HDD\_M2

**2280 SSD NGFF slot C Key M**

+3.3V\_HDD\_M2

JNGFF3\_CONN@

<10> PCIE\_PRX\_DTX\_N13  
<10> PCIE\_PRX\_DTX\_P13  
<10> PCIE\_PT\_X\_DRX\_N13  
<10> PCIE\_PT\_X\_DRX\_P13  
<10> PCIE\_PRX\_DTX\_N14  
<10> PCIE\_PRX\_DTX\_P14  
<10> PCIE\_PT\_X\_DRX\_N14  
<10> PCIE\_PT\_X\_DRX\_P14  
<10> PCIE\_PRX\_DTX\_N15  
<10> PCIE\_PRX\_DTX\_P15  
<10> PCIE\_PT\_X\_DRX\_N15  
<10> PCIE\_PT\_X\_DRX\_P15  
<10> PCIE\_PRX\_DTX\_N16  
<10> PCIE\_PRX\_DTX\_P16  
<10> PCIE\_PT\_X\_DRX\_N16  
<10> PCIE\_PT\_X\_DRX\_P16

+3.3V\_HDD\_M2 @RN37

M2280\_DEVSLP 10K\_0402\_5%

if signal is PCIE GEN3/SATA GEN3 maybe change C value or no need for DG0.9 SATA EXPRESS HDD

<11> CLK\_PCIE\_N2  
<11> CLK\_PCIE\_P2

<10> M2280\_PCIE\_SATA#

GND\_1  
GND\_2  
PERn3  
PERp3  
GND\_3  
PETp3  
PETn3  
GND\_4  
PERn2  
PERp2  
GND5  
PETp2  
PETn2  
GND6  
PERn1  
PERp1  
GND7  
PETn1  
PETp1  
GND8  
PERn0/SATA-B+  
PERp0/SATA-B-  
GND9  
PETn0/SATA-A-  
PETp0/SATA-A+  
GND10  
REFCLKN  
REFCLKP  
GND11

N/C\_19  
PEDET (OC-PCie/GND-SATA)  
GND\_12  
GND\_13  
GND\_14  
GND\_15  
NPTH\_2

LOTES\_APCI0170-P001A

Link APCI0170-P001A done 0123

+3.3V\_HDD\_M2

SSD\_SCP#\_R@RN1291  
NVME\_LED#  
@RN100

SSD\_SCP# <58>

PCH\_PLTRST#\_AND  
CLKREQ\_PCIE#2 <11>  
PCIE\_WAKE# <42,52,59>

SUSCLK\_R@RN99 1 2 0 0201\_5% <> SUSCLK <11,52>

+3.3V\_SSD from SSD storage protection power gate control

0212 change RN130 covering green printing for co-lay materials

RN131  
JUMP@ PJP31  
PAD\_OPEN1x3m  
RN130

0.01\_0805\_1% +3.3V\_RUN

0.01\_0805\_1%

0.0201\_5%

0.0201\_5%

DEVSLP N/C\_12 N/C\_13 N/C\_14 N/C\_15 N/C\_16 PERST# CLKREQ# PEWake# N/C\_17 N/C\_18

DAS/DSS# 3.3VAUX\_3 3.3VAUX\_4 3.3VAUX\_5 3.3VAUX\_6 N/C\_3 N/C\_4 N/C\_5 N/C\_6 N/C\_7 N/C\_8 N/C\_9 N/C\_10 N/C\_11

DELTA Confidential/Proprietary

Compal Electronics, Inc.

**M2 2280 Socket LA-G871P**

Title  
Size Document Number  
Date: Tuesday, March 05, 2019 Sheet 68 of 109

Rev 1.0


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[illegible][illegible]



# Reserve

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**DELL CONFIDENTIAL/PROPRIETARY**

**Compal Electronics, Inc.**

Title

**eMMC / UFS**

Size Document Number

**LA-G871P**

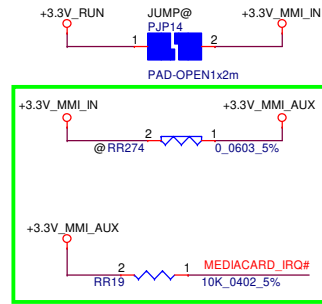
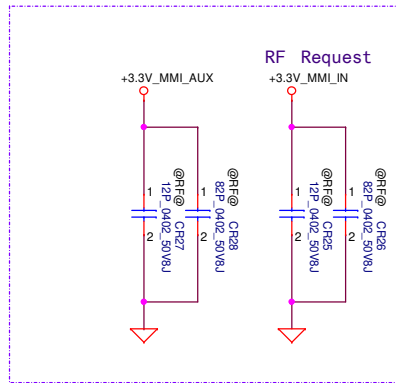
Date: Tuesday, March 05, 2019

Rev

1.0

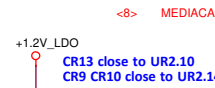
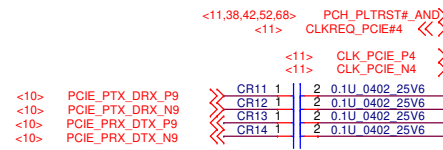
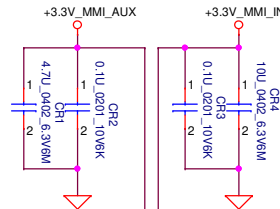
Sheet 69 of 109

# For PCIE Interface



support D3 Hot(if D3 cold PIN11,PIN27 need Add MOS on/off 3V3AUX)

7/18 Vender suggest.

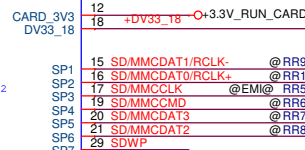
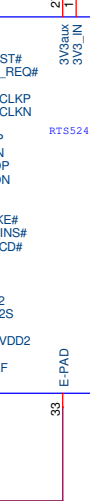


CR13 close to UR2.10  
CR9 CR10 close to UR2.14

+1.8V\_RUN\_CARD

+RREF

6.2K 0402 1%



7/18 Vender suggest

SD/MMCCD+

SD/MMCCD-

SD/MMCCD+

SD/MMCCD-

SD/MMCCD+

SD/MMCCD-

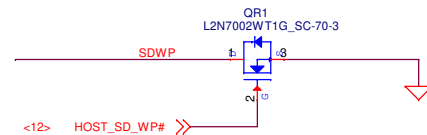
SD/MMCCD+

SD/MMCCD-

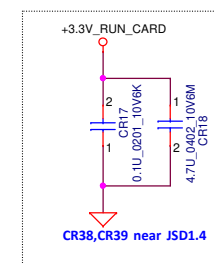
SD/MMCCD+

SD/MMCCD-

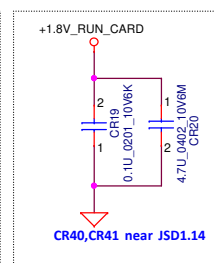
HOST_SD_WP#	SDWP	STATUS
High	Low	Write Enable
Low	High	Write Protect(FW LOCK)



<12> HOST\_SD\_WP#



CR38,CR39 near JSD1.4



CR40,CR41 near JSD1.14

+3.3V\_RUN\_CARD

+1.8V\_RUN\_CARD

SD/MMCCD+

SD/MMCCD-

SD/MMCCD+

SD/MMCCD-

SD/MMCCD+

SD/MMCCD-

SD/MMCCD+

SD/MMCCD-

SD/MMCCD+

SD/MMCCD-

SD/MMCCD+

SD/MMCCD-

SD/MMCCD+

SD/MMCCD-

SD/MMCCD+

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SD/MMCCD+

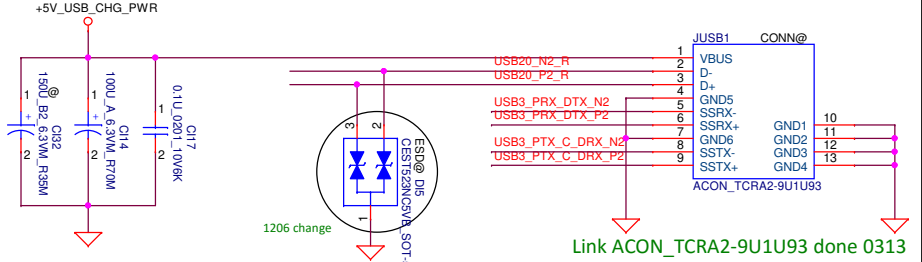
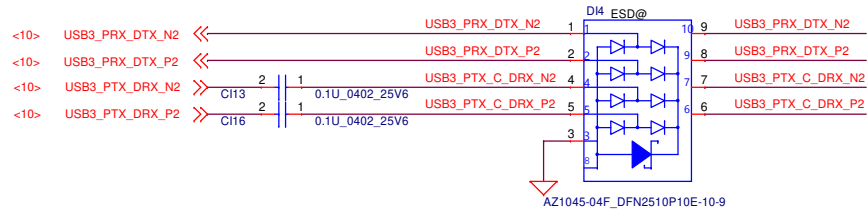
SD/MMCCD-

SD/MMCCD+

SD/MMCCD-

SD/MMCCD+

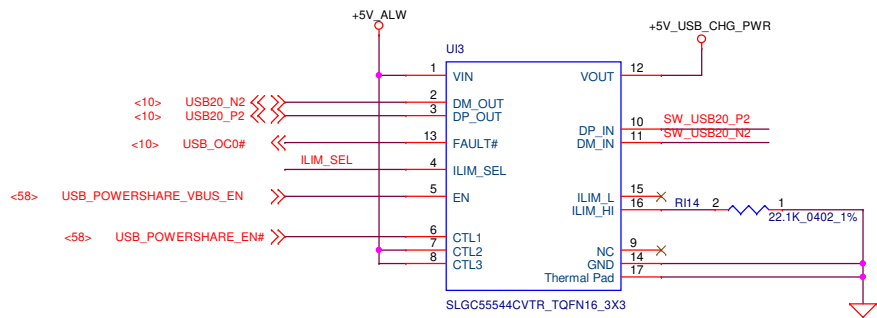
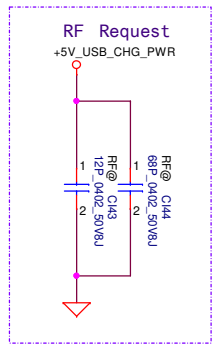
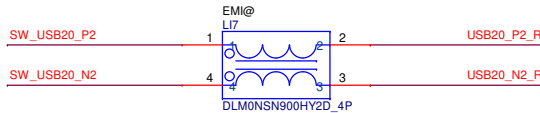
For Merion 14



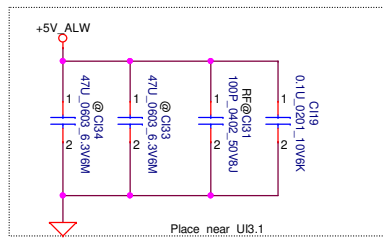
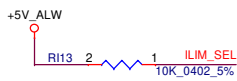
Link ACON\_TCRA2-9U1U93 done 0313

Merion Limit height  
DI5 change to H=0.9mm(MAX)

Merion14 swap LI7 net for layout routing



Link Seligro SA000097E10 Done  
MAIN : SLGC55544CVTR



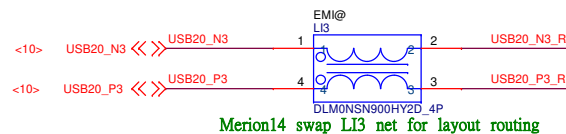
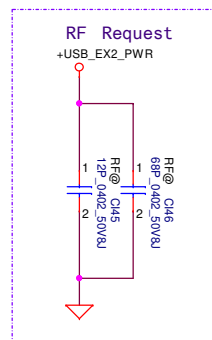
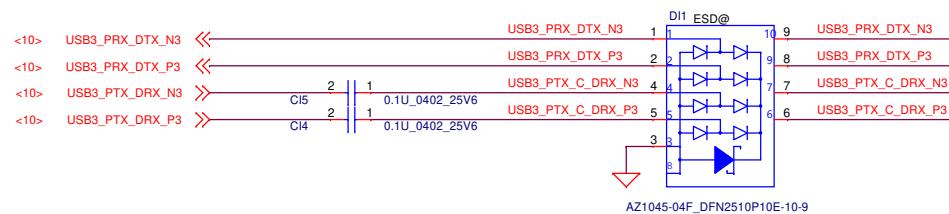
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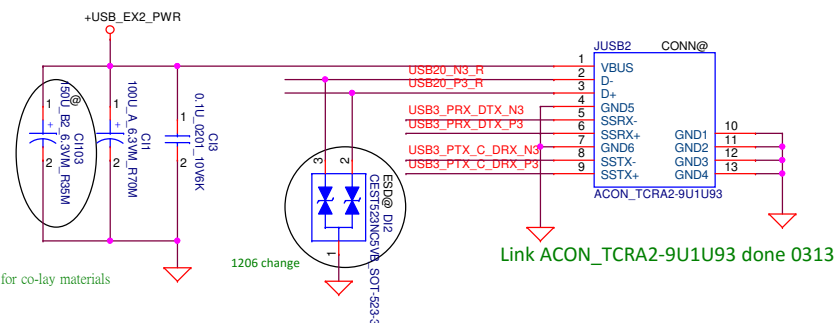
Title		JUSB1+PS
Size	Document Number	LA-G871P
Date:	Tuesday, March 05, 2019	Sheet 71 of 109

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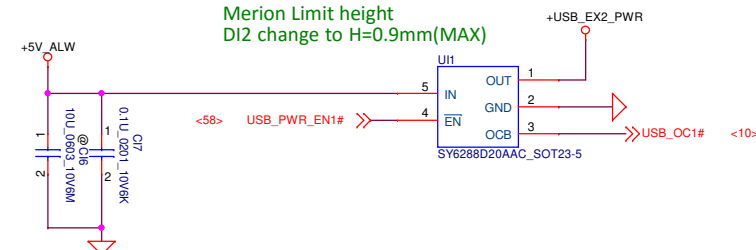


DFB request:  
main SM070003Z00 (INPAQ\_MCM1012B900F06BP\_4P)  
Footprint use 2nd source SM070004400 (PANAS\_EXC24CQ900U\_4P)  
Pitch change from 0.5mm to 0.55mm

0212 change  
CI103 covering green printing for co-lay materials



Merion Limit height  
DI2 change to H=0.9mm(MAX)



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Title		JUSB2	Rev 1.0
Size	Document Number	LA-G871P	
Date:	Tuesday, March 05, 2019	Sheet 72 of 109	

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Title **USB2/USB3 DB**

Size	Document Number	Rev
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Date: **Tuesday, March 05, 2019** Sheet **73** of **109**


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Dock			
Size	Document Number		Rev
	LA-G871P		1.0
Date:	Tuesday, March 05, 2019		Sheet 74 of 109

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Reserve for USB

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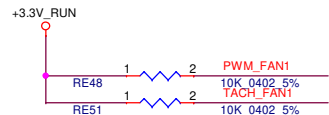
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# Reserve

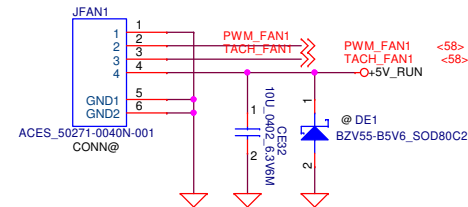
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Title		
Reserve for USB		
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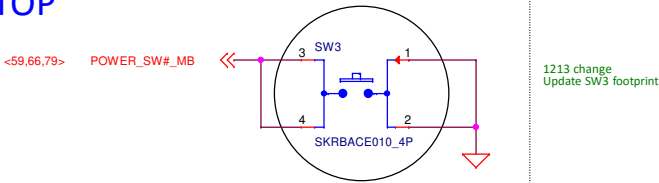


Link 50271-0040N-001 done 0123



Fan follow X9 project PIN DEFINE

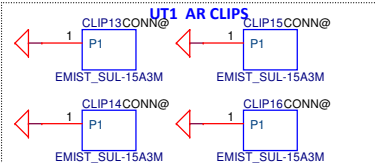
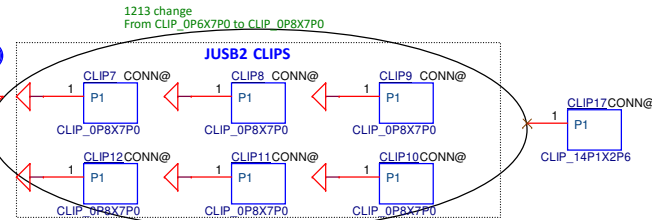
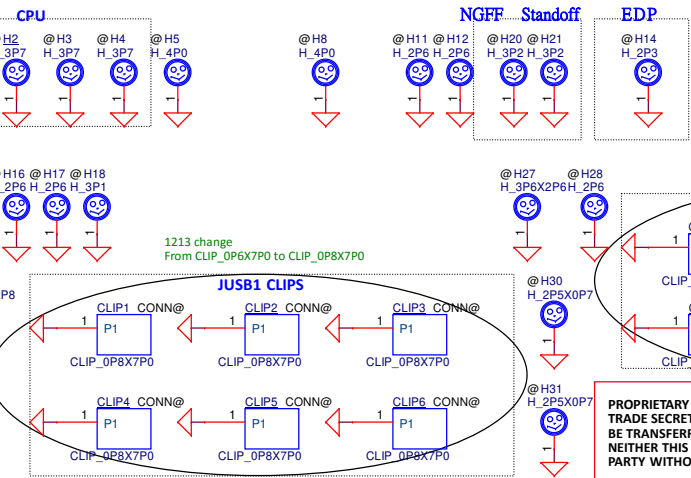
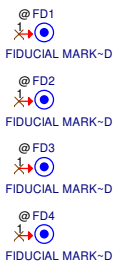
# POWER & INSTANT ON SWITCH TOP



LED Circuit Control Table

	LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

## Fiducial Mark



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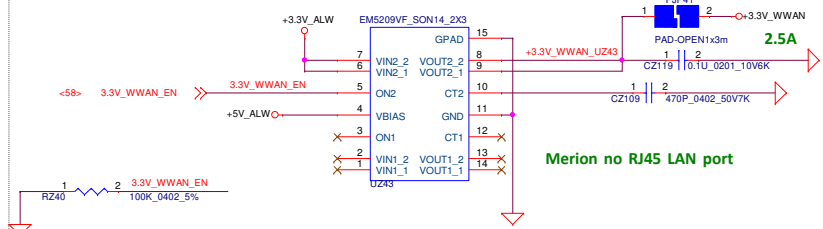
**PWRBTN, PAD, ME, FAN**

**LA-G871P**

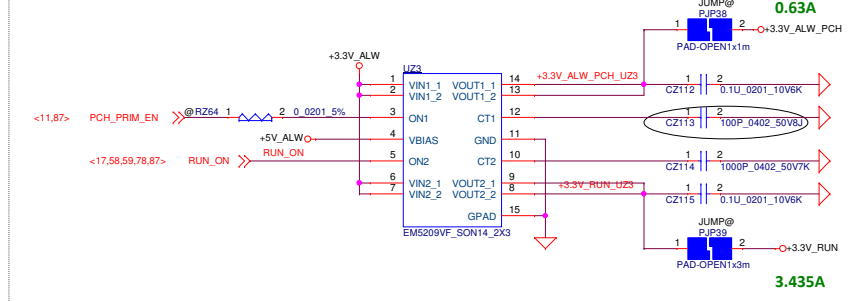
Title	PWRBTN, PAD, ME, FAN		Rev	1.0
Size	Document	Number		
Date:	Tuesday, March 05, 2019	Sheet	77	of 109

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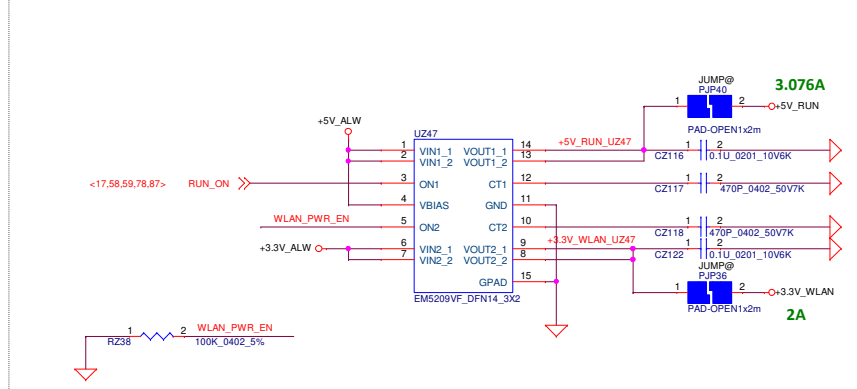
### +3.3V\_WWAN/+3.3V\_LAN source



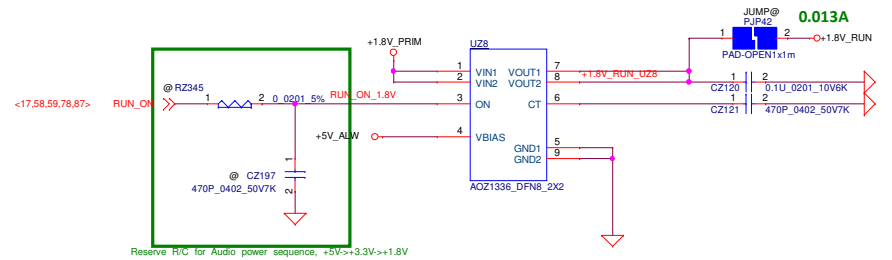
### +3.3V\_ALW\_PCH/+3.3V\_RUN source



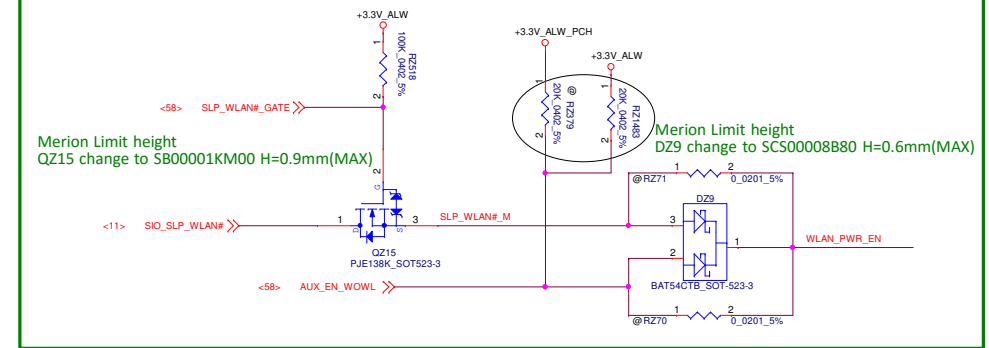
### +5V\_RUN/+3.3V\_WLAN source



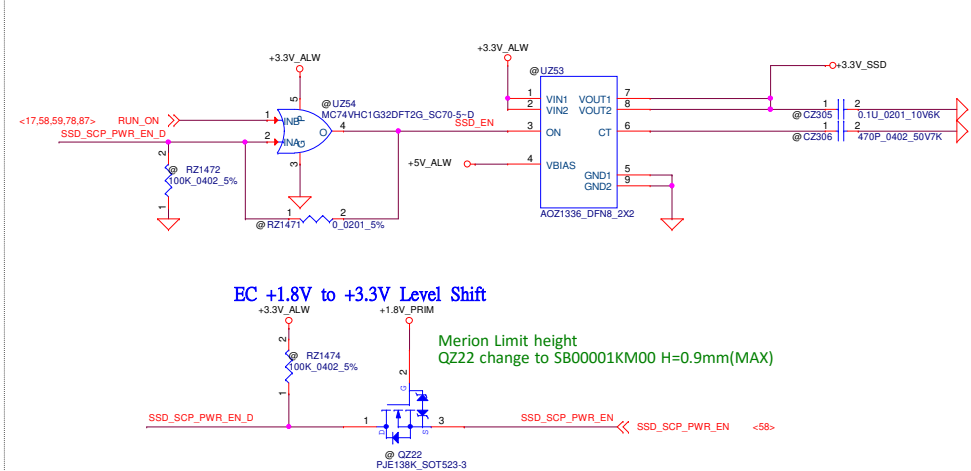
### +1.8V\_RUN source



EC request to reserve OR gate for WLAN power enable



Reserve for SSD storage protection power gate control Reference Berlinetta CFL pilot



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Power control

LA-G871P


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Google Debug & INAs

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Rev

1.0



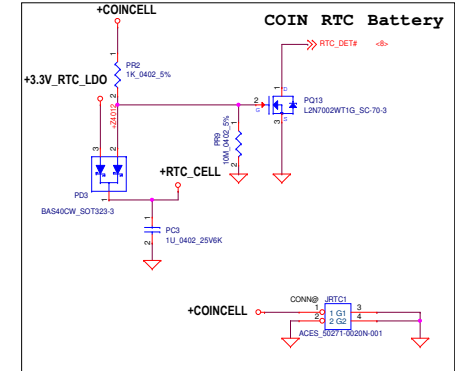
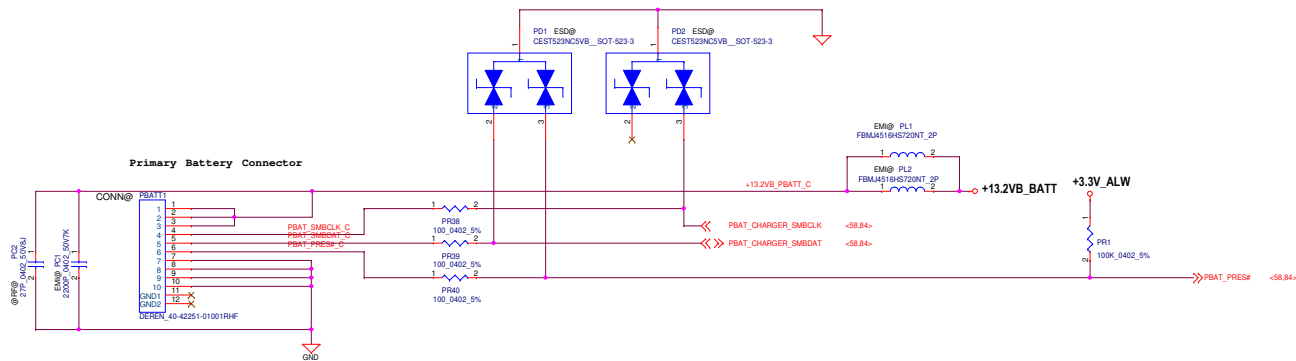
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Title <b>PWR-Block Diagram</b>		
Size	Document Number <b>LA-G871P</b>	Rev 1.0
Date: <b>Tuesday, March 05, 2019</b> Sheet <b>81</b> of <b>109</b>		





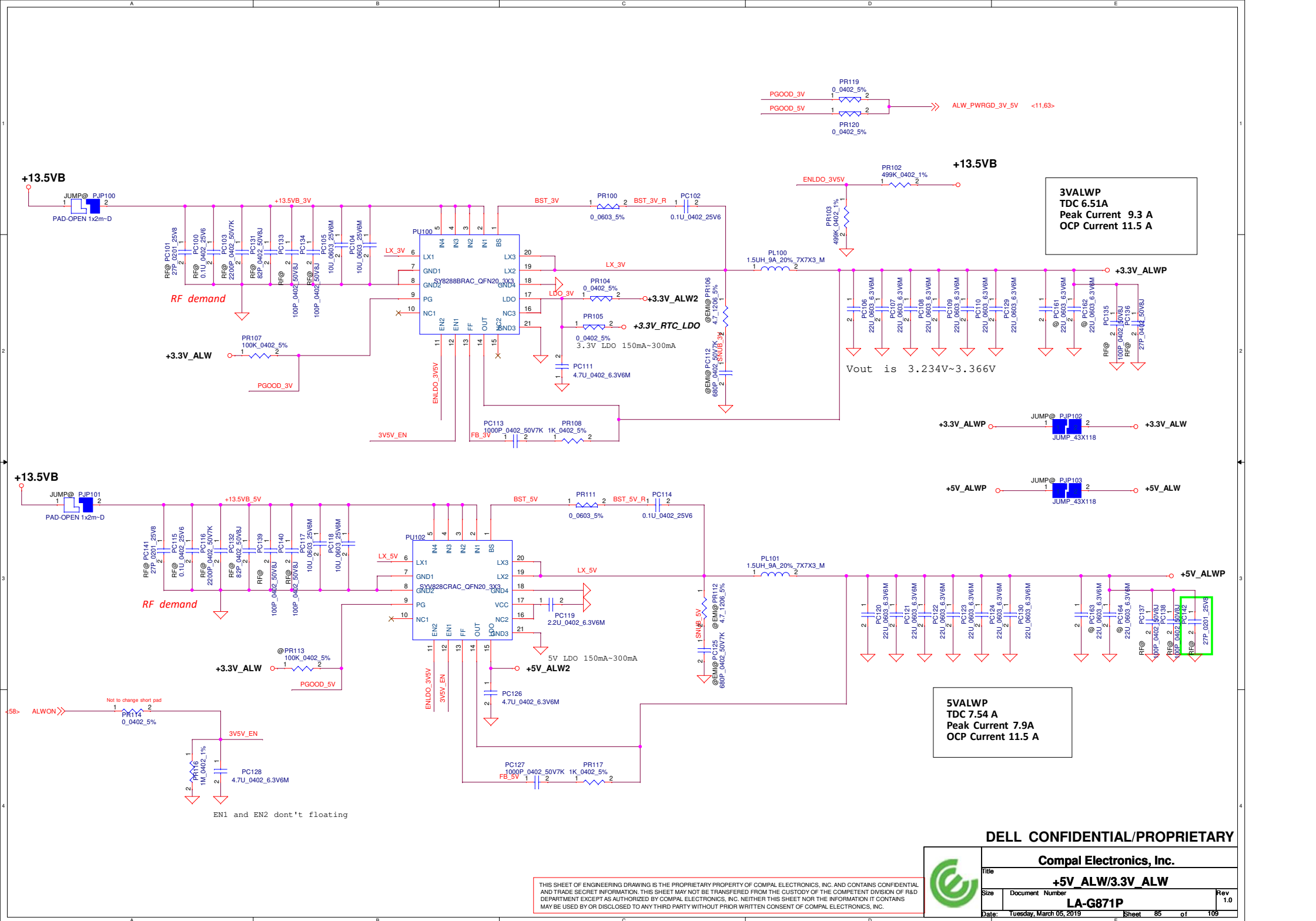
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		Compal Electronics, Inc.	
		Battery Connector/ RTC	
Rev	Document Name	LA-G871P	
Date	Issued	March 05, 2019	Sheet 83 of 109

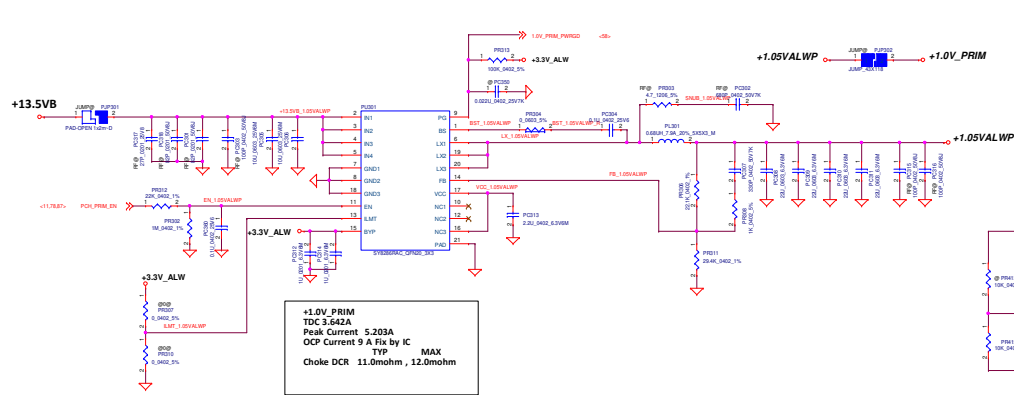
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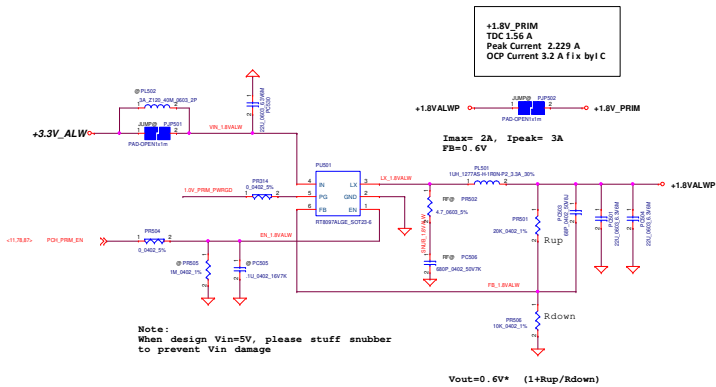




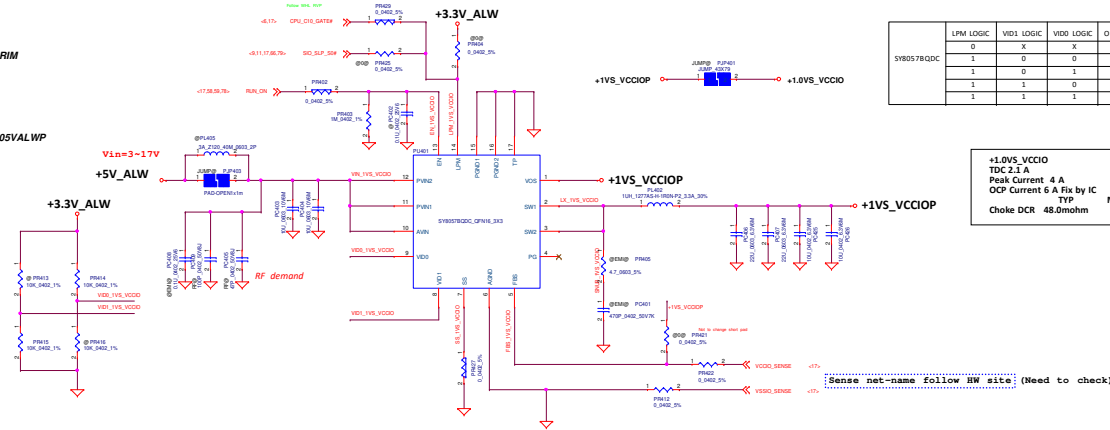
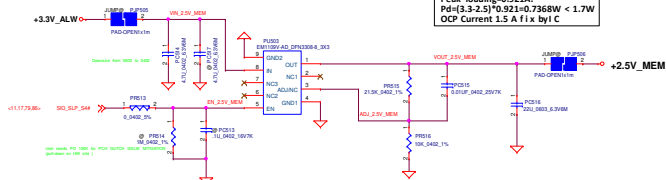




The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high

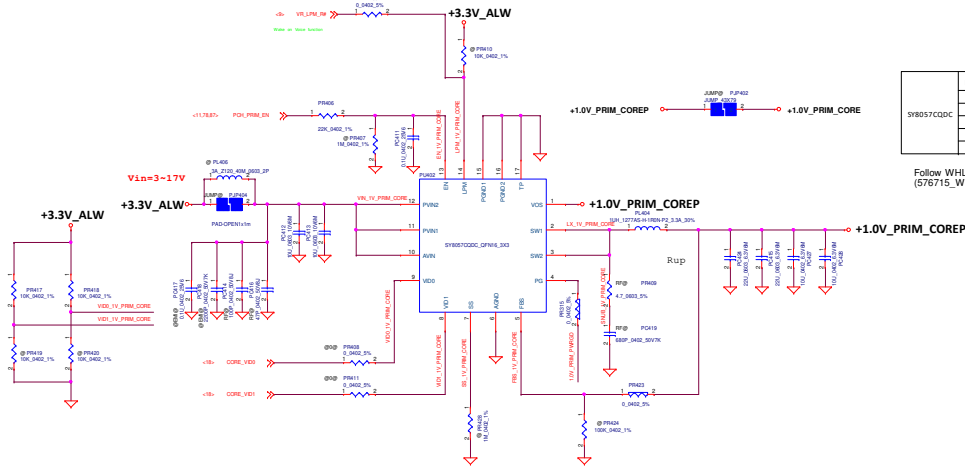


**+2.5V MEM**  
TDC 0.645A by power budget  
AP7361 U-DNR0300-8 f<sub>ld</sub> limit=1.7W  
Peak loading=0.921A  
P<sub>ld</sub>=(3-2.5)\*0.921=0.736W < 1.7W  
OCP Current 1.5 A fix by C



LPM LOGIC	VDD1 LOGIC	VDD0 LOGIC	OUTPUT VOLTAGE
0	X	X	0.75(LPM)
1	0	0	0.9
1	0	1	0.95
1	1	0	1.00
1	1	1	1.05

Follow WHL  
(S76715\_WHL\_U\_DDR4\_HDK\_HW\_Design\_Kit\_Rev0p5)



**+1.0V PRIM\_CORE**  
TDC 2.237 A  
Peak Current 3.195A  
OCP Current 6.8 A fix by IC  
TYP MAX  
Choke DCR 48.0mohm

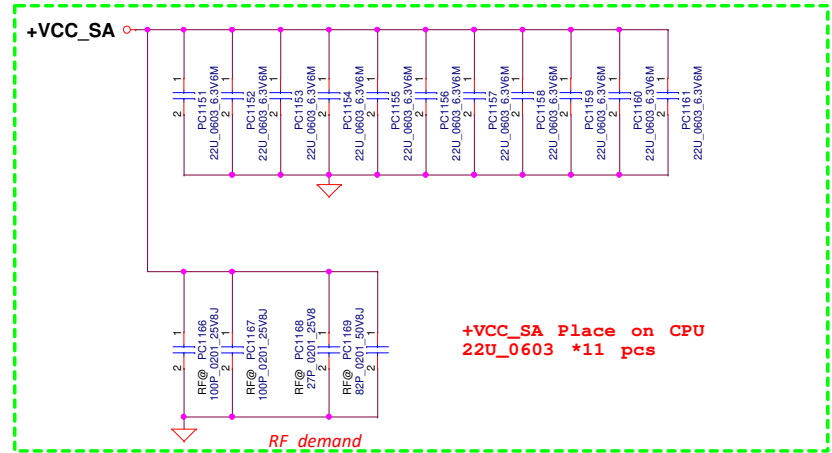
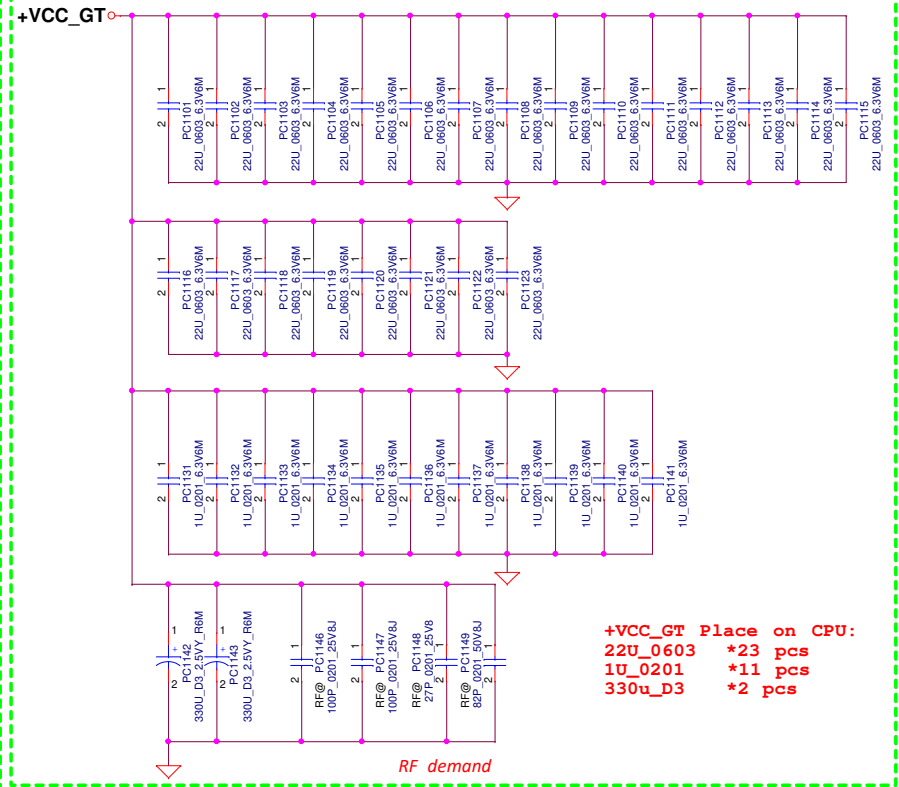
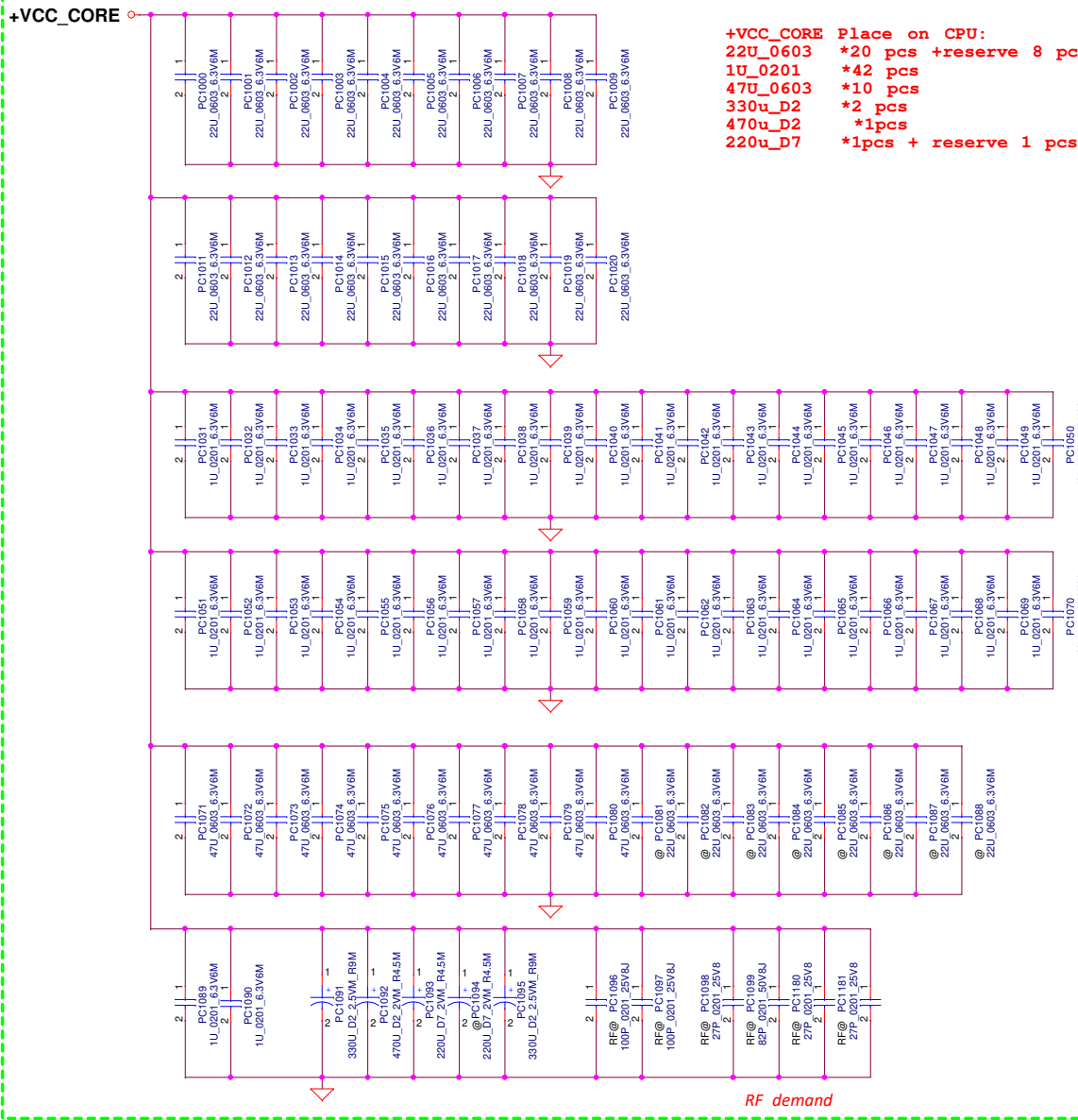
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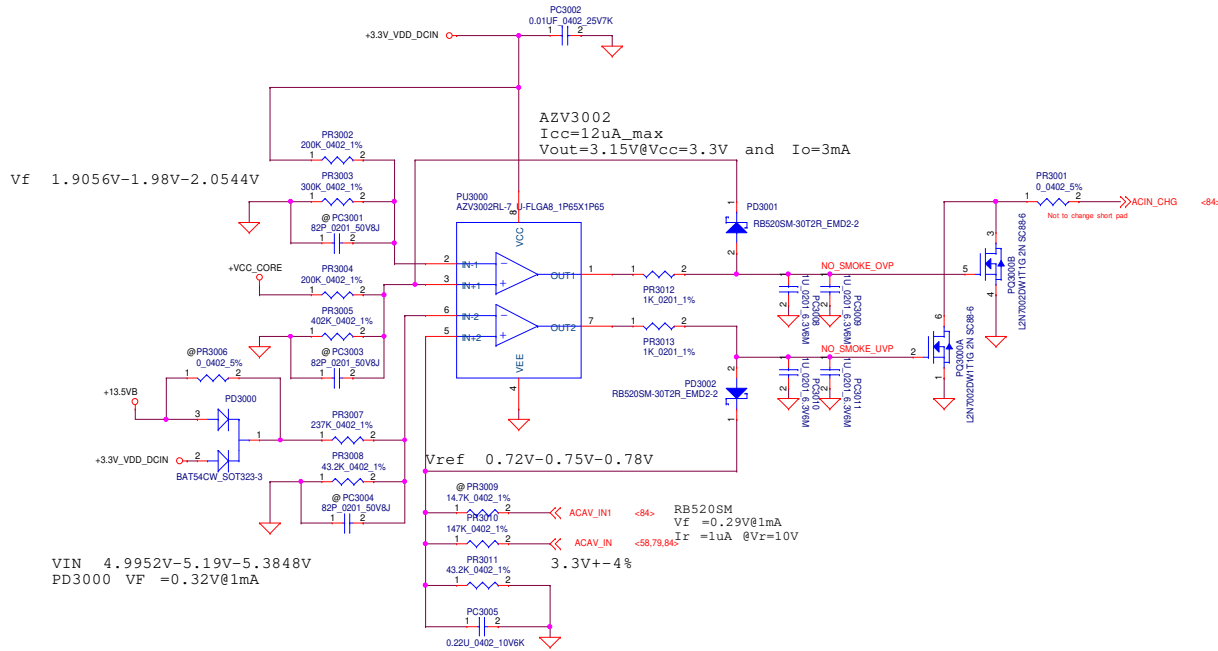


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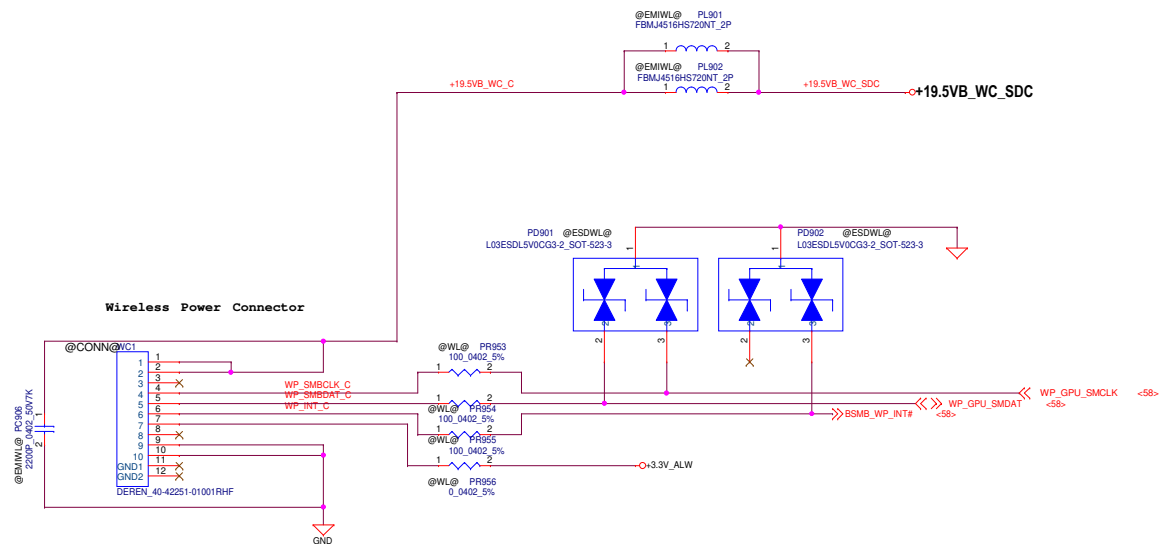
Compal Electronics, Inc.		
CPU Decoupling CAP		
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Charger UVP/VCORE OVP			
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Reserve for PWR			
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U42

PC626 U42@ 	PR613 U42@ 	PR621 U42@ 	PC624 U42@ 
0.1U_0402_25V6	97.6K_0402_1%	316_0402_1%	0.022U_0402_16V7K
PR638 U42@ 	PR622 U42@ 	PC616 U42@ 	PC617 U42@ 
523_0402_1%	2.49K_0402_1%	68P_0402_50V8J	1200P_0402_50V7K

U22

PC626 U22@ 	PR613 U22@ 	PR621 U22@ 	PC624 U22@ 
0.047U_0402_25V7K	84.5K_0402_1%	316_0402_1%	0.033U_0402_25V7K
PR638 U22@ 	PR622 U22@ 	PC616 U22@ 	PC617 U22@ 
422_0402_1%	1.65K_0402_1%	33P_0402_50V8K	1200P_0402_50V7K

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BOM Option			
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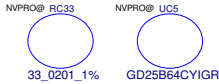
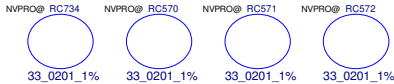
Version Change List ( P. I. R. List )				Issue Description	Solution Description	Rev.
Item	Page #	Date				
1	P089	06/04	Fairchild & AOS Dr.MOS vendor remove PVCC reserved resistors	Delete reserved PR686/PR689/PR681 on PVCC side	X01	
2	P082 P086 P088 P089	06/08 07/02	Change to common P/N	1. PC624 change to SE076223K80 (S CER CAP 0.022U 16V K X7R 0402) 2. PC804 change to SE074221K80 (S CER CAP 220P 50V K X7R 0402) 3. PC633 change to SE075472K80 (S CER CAP 4700P 25V K X7R 0402) 4. PL201 change to SH00000YE00 (common P/N) 5. PL614 change to SH00001ED00 (common P/N)	X01	
3	P090	07/12	Merion Top side Z-height limitation	1. Un-stuff PC1094 (@) 2. Add stuff PC1095 - 330uF (Bottom side)	X01	
4	P088 P099	07/13	CPU intel validation form test tune value	1. Change the PR636 from 665 Ohm to 634 Ohm. - (VCCSA Ri) -> SD00000Z280, S RES 1/16W 634 +-1% 0402 2. Change the PR640 from 374 Ohm to 365 Ohm. - (VCCGT Ri) -> SD034365080, S RES 1/16W 365 +-1% 0402 3. Change the PC646 from 0.047uF to 0.0022uF. - (VCCGT RC) -> SE075222K80, S CER CAP 2200P 25V K X7R 0402 4. Change the PC642 from 0.033uF to 0.068uF. - (VCCGT RC) -> SE000003J80, S CER CAP 0.068U 16V K X7R 0402 5. Change the PC621 from 680pF to 820pF. - (VCCIA FB RC). -> SE000008980, S CER CAP 820P 25V K X7R 0402 6. Change the PR611 from 1.87kOhm to 9.31kOhm. - (PROG2) -> SD034931180, S RES 1/16W 9.31K +-1% 0402	X01	
5	P082 P083	07/20	ESD request	PD1, PD2, PD4 change to SCA00002A00 for ESD demand	X01	
6	P082	07/30	LPS function test fail on G3 mode. Need to return LDO(PU2) design circuit.	Need stuff item : PU2/ PC10/ PC11/ PR47/ PR33/ PR27/ PR17/ PD800 / PR806 / PR809/ PR832/ PR859 / PR810 / PR813 Need delete location : PR48 / PR34 / PR35 / PR36 / PR37/ PR847 / PR848 / PR849/ PR850 Need un-stuff item : PR851 / PR860 / PR852	X01	
7	P082	07/30	PQ8 gate for Back drive issue	Add R/C delay PR865/PC865 : 100K(SD028100380) and 0.1uF_0402_25V(SE00000G880)	X01	
8	P082	08/10	LM393 resistor value fine tune	PR800 change to 422K_0402_1% (SD034422380) PR815 change to 37.4K_0402_1% (SD034374280) PR832 change to 102K_0402_1% (SD028102380) PR843 change to 37.4K_0402_1% (SD034374280) PR831 change to 1M_0402_1% (SD034100480) PR842 change to 191K_0402_1% (SD034191380)	X01	
9	P088	08/10	ISL95857 CPU Controller change to Rev.C	PR651 value change to 39.2K for ISL95857C	X01	
10	P082 P083	08/15	Follow Schematic naming rule	Re-define the RTC/DCIN/Battery connector from @ to CONN@.	X01	
11	P082 P083	08/15	Check and modify connector P/N for ME request	PJPCD1 - SP02001A500 PBATT1 - SP02001A700 JRTC1 - SP02000R000	X01	
12	P087	08/15	R/C delay fine tune for WHL bring up sequence	1. Modify PR312 / PR406 value from 0 ohm to 22K_0402_1% (SD034220280) 2. PC411 change to stuff 3. Add PC360 : 0.1uF_0402_25V (SE00000G880)	X01	
13	P091	08/20	Remove double pull down resistor	Un-stuff PR505 / PR407	X01	
14	All	08/20 08/30	RF request	1. PC301 pop & change from 0.1u to 82pF 2. PR502/PC506 change to pop (Snubber not to downsize) 3. PC1096/PC1097 change to pop 4. PC1166/PC1167 change to pop 5. PC1146/PC1147 change to pop 6. Add PC101 27pF for RF +3.3V input 7. Add PC141 27pF for RF +5V input 8. Add PC230 27pF, PC231 100pF for RF +1.2V_DDR input 9. Add PC317 27pF, PC318 82pF for RF +1.05V_ALWP input 10. Add PC609 27pF, PC610 82pF for RF +VCC_SA input 11. Add PC689 27pF, PC690 82pF for RF +13.5VB_CPU input 12. Add PC691 27pF, PC692 82pF for RF +13.5VB_VCCGT input 13. Add PC1098 27pF, PC1099 82pF for RF +VCC_CORE input 14. Add PC1148 27pF, PC1149 82pF for RF +VCC_GT input 15. Add PC1168 27pF, PC1169 82pF for RF +VCC_SA input 16. Add PC756,PC759 (22pF)/ PC757, PC760 (47pF)/ PC758, PC761 (100pF) 17. Reserve PC2 (27pF) 18. Add PC1180, PC1181 (27pF)	X01	
15	P083	08/21	RTC issue for HW request	Add RTC detect circuit 1. Add PR9 10Mohm 2. Add PQ13 MOS	X01	
16	P091	08/22	Charger UVP & VCORE OVP circuit	Add Charger UVP & VCORE OVP circuit	X01	
17	P082	08/22 09/11	LPS function modify	1. Add un-stuff PR870 and pull up source is +20V_VBUS_DC_SS ; 499K_0402_1% (SD034499380) 2. Modify PR831 value to 499K_0402_1% (SD034499380) and pull up source change to +20V_TBTA_VBUS_1 3. Modify PR842 value to 97.6K_0402_1% (SD034976280) 4. PC811 change to SE00000UD00 (10U 6.3V M X5R 0402)	X01	
18	P082	08/22	Modify 1 barrel / 1 Type-C External LDO circuit for Charger UVP & VCORE OVP circuit design	1. PD800 change to un-stuff 2. Add PR866_0_0402_5% 3. Add PD803 (BAT54CW_SOT323-3) 4. Add un-stuff PR868_0_0603_5%	X01	
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Version Change List ( P. I. R. List )					
Item	Page #	Date	Issue Description	Solution Description	Rev.
19	P088 P089	08/22	CPU VR input Low noise MLCC PCB footprint update : C_0603-S3	IA input : PC658 / PC657 / PC656 / PC682 / PC683 / PC684 / PC672 / PC673 GT input : PC675 / PC674 / PC664 / PC665 SA input : PC612 / PC608 IA output : PC1071 / PC1072 / PC1073 / PC1074 / PC1075/ PC1076 / PC1077 / PC1078 / PC1079 / PC1080	X01
20	P090	08/22	Un-stuffed CPU +VCC_CORE output MLCC change value	Change reserve location from 47uF to 22uF (Keep un-stuff) PC1081 / PC1082 / PC1083 / PC1084 / PC1085 / PC1086 / PC1087 / PC1088	X01
21	P089	08/22	Remove double net name	Remove PU610 / PU612 / PU613 Dr.MOS pin 15(PVCC) double net name	X01
22	P087	08/23	Change PU301, PU501 powergood connection netname	Change connection to 1.0V_PRIM_PWRGD from 1.8V_PRIM_PWRGD (PU301, PU501)	X01
23	P087	08/28	R/C for WHL sequence	1. Add PR313 : 100K_0402_5% 2. Add PR314 / PR315 : 0 ohm ( 3. Reserve PC350 footprint to PG (1.0V_PRIM_PWRGD) signal	X01
24	P089	08/28	1 barrel / 1 Type-C change solution 2	Change to Stuff : PR46 / PR41 / PR858 / PR857 / PQ12 / PR49 / PQ814 / PR861 Un-stuff : PR856 / PR43	X01
25	P091	09/04	Disable Charger UVP & VCORE OVP function	Un-stuff PR3001 for disable No Smoke function	X01
26	P090	09/14	DCIN AC detect tune value	Change PR817 to SD034249280 (S RES 1/16W 24.9K +-1% 0402)	X01
27	All	09/11	Follow schematic naming rule	Jump BOM structure change Solder -> JUMP@ Not Solder -> @JUMP@	X01
1	P091	11/05	Charger UVP/VCORE OVP circuit	1. PR3002 change to 200K_0402_1% (SD034200380) 2. PR3003 change to 300K_0402_1% (SD034300380) 3. PR3001 change to stuff 4. Add PC3008 / PC3009 on NO_SMOKE_OVP 5. Add PC3010 / PC3011 on NO_SMOKE_UVP	X02
2	P084 P088	11/05	Charger IC PU700 & CPU Controller IC PU602 change P/N for MP	1. PU700 change P/N to SA0000BWG0L for MP 2. PU602 change P/N to SA0000BYJ0L for MP	X02
3	P090	11/05	Barrel & typeC B2B MOSFET P/N change	1. Check PQ4/PQ801/PQ702 1st parts is SB00001MT00 (SB00001MT00 - AONR21357 1P DFN3X3-8) . 2. PQ9 / PQ800 CPN change to SB00001BX1L (EMZB08P03V 1P EDFN3X3-8)	X02
4	All	11/28	0 ohm short pad total 69 pcs	PR19, PR20, PR22, PR25, PR861, PR42, PR44, PR46, PR47, PR49, PR100, PR104, PR105, PR111, PR119, PR120, PR203, PR208, PR210, PR304, PR314, PR315, PR402, PR423, PR504, PR513, PR602, PR603, PR606, PR614, PR616, PR620, PR625, PR659, PR662, PR664, PR679, PR687, PR709, PR713, PR715, PR719, PR721, PR722, PR727, PR729, PR731, PR736, PR737, PR740, PR741, PR743, PR814, PR816, PR818, PR820, PR826, PR827, PR829, PR834, PR836, PR840, PR844, PR853, PR854, PR858, PR859, PR671, PR692	X02
5	P082	11/28	Barrel & typeC B2B control circuit	Change to un-stuff parts : PC13 / PU3 / PR45 / PC814 / PU801 / PR855	X02
6	P084 P089	12/03	Add " -NPM " PCB Footprint to cover green paint for Co-lay Depop Component.	PJP700 -> JUMP_43X118-NPM PL602 -> 9A_280_1812_2P-NPM	X02
7	P082	12/04	ESD Request	PD1, PD2 change P/N to SCA00004700, S ZEN ROW CEST523NC5VB 3P C/A SOT-523 AU Due to AMZ SCA00002X00 has be removed in ESD common pool	X02
8	P082	12/12	PD803 voltage derating back up solution	1. Remove PR868 reserve 0ohm 2. Add PR892 / PR893 for PD803 voltage derating back up solution. SD002220A80 - S RES 1/8W 22 +-5% 0805 3. PD803 Pin 1 add net name : +20V_LDO_INPUT	X02
9	P084	12/13	Charger input current sense R for more quickly sensing	PR701 / PR702 change to 1_0603_1% (SD014100B80) for more quickly sensing	X02
10	P091	12/13	Charger UVP/VCORE OVP circuit	1. PR3010 change value from 14.7K to 147K(SD034147380) for more sequence margin. 2. PR3011 change value from 4.32K to 43.2K(SD034432280) for more sequence margin.	X02
11	P085 P086	12/13	RF Request	Add PC228 27pF on +1.2VDDRP, PC142 27pF on +5V_ALWP for RF demand	X02
12	P087	12/28	+1.0VS_VCCIO change from local sense to remote sense	1. PR421 change to depop (@0@) 2. PR412, PR422 change to pop	X02
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**Compal Electronics, Inc.**

**Bom option**

**LA-G871P**

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Version Change List ( P. I. R. List )			Issue	Solution	
Item	Page#	Date	Description	Description	Rev.
1	All	2018/07/23	Updated page define according to Dell request	Updated page define according to Dell request.	0.2 (X01)
2	79	2018/07/23	1.Modified QZ3 footprint to correct 2.Modified parts pin define to correct	1.Change QZ3 footprint to SOT-323 from SOT-23. 2.Change SW1 pin define.	0.2 (X01)
3	09	2018/07/23	Modified parts pin define to correct	Change JASA1 pin define (swap pin1&4, pin2&3).	0.2 (X01)
4	44	2018/07/23	1.Modified parts location to align with X9 2.Change PD controller to 65982DD	1.Change CT358 location to CT82. 2.Change UT5 part to SA0000C800 from SA0000BIJ00.	0.2 (X01)
5	11	2018/07/23	RTC elapsed time can not meet the Spec (spec: +/- 2 secs)	Change CC23, CC26 part to 15P_0402_50V8J from 12P_0402_50V8J.	0.2 (X01)
6	50	2018/07/23	1.Modified parts BOM Structure 2.Modified layout Limit height problem	1.Change RC24 BOM Structure to @NVPRO from @. 2.Change QC2 part to SB000014X00 from SB00000PV00.	0.2 (X01)
7	52	2018/07/23	Modified parts pin define to correct	Change JANT1, JANT2 pin define (swap pin1&5, pin2&4).	0.2 (X01)
8	102	2018/07/23	Modified NVPRO BOM option RZ58~RZ60 to correct	Change RZ58~RZ60 BOM option part to 33_0402_1% from 33_0201_1%.	0.2 (X01)
9	56	2018/07/23	Modified according to ESD request	Change DA2 part to SCA00001A00 from SC600001600.	0.2 (X01)
10	66	2018/07/23	1.Modified layout Limit height problem 2.Change ST TPM to ST33HTPH2032AHC1 (MP version) 3.Add FPR_RST# pull high, align with merion13	1.Change DZ11 part to SCA00002A00 from SCA00001B00. 2.Change UZ12 part to SA0000C5G10 from SA00009SO40. 3.Add RZ1392 (100K_0201_5%) pull high to +3.3V_FPBTN.	0.2 (X01)
11	59	2018/07/23	Modified layout Limit height problem	Change UE4 part to SA00007YE00 from SA00007WE00.	0.2 (X01)
12	78	2018/07/23	Modified layout Limit height problem	Change DZ9 part to SCS00008B80 from SCS00006400. Change QZ15, QZ22 part to SB00001KM00 from SB00000VD00.	0.2 (X01)
13	14	2018/07/23	Modified layout Limit height problem	Change QC4 part to SB000014X00 from SB00000PV00.	0.2 (X01)
14	38	2018/07/23	Modified layout Limit height problem	Change QV2, QV7 part to SB00000NK00 from SB00000UO00.	0.2 (X01)
15	40	2018/08/09	1.Modified layout Limit height problem 2.Modified parts according to EMI & EE test result	1.Change QV4, QV5 part to SB00000NK00 from SB00000UO00. 2.Change RV26, RV29, RV32, RV35 part to 130_0402_5% from 300_0402_5%. Change LV31~38 to 5.6_0402_5% from SHI00006Q00. Change LV31~38 location to RV56~RV63.	0.2 (X01)
16	79	2018/08/09	1.Dell request to modify M_BIST circuit 2.Modified parts to correct capacitance voltage 3.Delete unnecessary parts, align with X10 projects	1.Change netname to M_BIST from M_BITS. Change RZ1413 part to SD028330380 (330K_0201_5%) from SD00000HX80 (221K_0201_1%). Add location RZ1482 (1M_0402_5%) pull up to +3.3V_ALW. Change RZ1413, DZ12 to depop from pop. 2.Change CZ218 part to SE00000UC00 (1U_0201_6.3V6M) from SE000013500 (1U_0201_10V6M). 3.Delete location RV632 (0_0402_5%).	0.2 (X01)
17	18	2018/08/09	1.Modified parts downsize according to Intel confirmed 2.Modified parts according to Intel BSOD issue recommend 3.Reserved WHEA circuit 4.Reserved WHEA R/C Filter circuit	1.Change CC65, CC66, CC73, CC75, CC98, CC1463, CC1464, CC67, CC80, CC83 part to SE00000UC00 (1U_0201_6.3V6M) from SE000000K80 (1U_0402_6.3V6K). Add location CC68, CC69, CC70 (1U_0201_6.3V6M). Change CC72 part to SE000000580 (0.1U_0201_6.3V6K) from SE095104K80 (0.1U_0402_10V6K). Delete location CC74 (0.1U_0402_10V6K). 2.Change LC1~LC3 part to SHI0000XL00 (2.2uH 0603 INDUC) from SM01000RR00 (0603 Bead). Change CC100, CC102 part to SE00000M000 (22U_0603_6.3V6M) from SE00001500 (47U_0603_6.3V6M). Add location CC103, CC104 (22U_0603_6.3V6M). Change LC2, LC3, CC100, CC102 to pop from depop. Change RC173, RC175 to depop from pop. 3.Delete location RC846 (0_0201_5%). Change CC85, CC86 part to SE00000M000 (22U_0603_6.3V6M) from SE000007280 (2.2P_0201_25V). Change LC1 BOM Structure to @ from @RF@. Change CC85, CC86 BOM Structure to @ from RF@. 4.Add location RC864 (0_0603_5%).	0.2 (X01)
18	58	2018/08/09	1.Modified according to GPIO map v1.4 2.Modified parts to correct capacitance voltage	1.Change netname to VCI_IN3# from NFC_ACTIVITY_STATUS#. Change netname to PTP_DISABLE# from TP_DISABLE#. 2.Change CE14, CE30, CE31, CE63 part to SE00000UC00 (1U_0201_6.3V6M) from SE000013500 (1U_0201_10V6M).	0.2 (X01)
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19	70	2018/08/09	Modified parts to correct capacitance voltage	Change CR15,CR22 part to SE00000UC00(1U_0201_6.3V6M) from SE000013500(1U_0201_10V6M) .	0.2 (X01)
20	08	2018/08/09	1.Change Non-Vpro UC6 ROM parts, align UC5 ROM parts vendor 2.Modified according to GPIO map v1.4	1.Change UC6 part to SA0000A8J10(GIGADEVICE) from SA00005VV20(WINBOND) . 2.Change netname to GPP_C2 from PCH_SMB_ALERT#.	0.2 (X01)
21	44	2018/08/09	Modified parts to correct capacitance voltage	Change CT83 part to SE00000UC00(1U_0201_6.3V6M) from SE000013500(1U_0201_10V6M) .	0.2 (X01)
22	06	2018/08/09	Modified netname to correct	Change netname to GPP_H23 from GPPC_H23.	0.2 (X01)
23	23	2018/08/09	1.Change parts follow sourcer request 2.Modified parts downsize according to Intel confirmed	1.Change CD25 part to SE000000580(0.1U_0201_6.3V6K) from SE095104K80(0.1U_0402_10V6K) . 2.Change CD9~CD16,CD18,CD19,CD23,CD24,CD69,CD70 part to SE00000UC00(1U_0201_6.3V6M) from SE000000K80(1U_0402_6.3V6K) .	0.2 (X01)
24	24	2018/08/09	1.Change parts follow sourcer request 2.Modified parts downsize according to Intel confirmed	1.Change CD57 part to SE000000580(0.1U_0201_6.3V6K) from SE095104K80(0.1U_0402_10V6K) . 2.Change CD41~CD48,CD50,CD51,CD55,CD56,CD71,CD72 part to SE00000UC00(1U_0201_6.3V6M) from SE000000K80(1U_0402_6.3V6K) .	0.2 (X01)
25	17	2018/08/09	Modified parts downsize according to Intel confirmed	Change CC28,CC29,CC31,CC430 part to SE00000UC00(1U_0201_6.3V6M) from SE000000K80(1U_0402_6.3V6K) .	0.2 (X01)
26	56	2018/08/09	1.Modified parts downsize according to RTK confirmed 2.Modified according to GPIO map v1.4 3.Modified AUX mode pin power rail to +3.3V_RTC_LDO 4.Modified parts to correct capacitance voltage 5.Modified smart amp. to support 3rd vendor	1.Change CA29,CA49 part to SE00000YB00(1U_0201_6.3V6K) from SE080105K80(1U_0603_10V6K) Add location CA76,CA77(1U_0201_6.3V6K) . 2.Change netname to SMART_SPK_DET0# from SPK_DET#. 3.Change RA53 to pop from depop. Change RA54 to depop from pop. 4.Change CA31 part to SE00000UC00(1U_0201_6.3V6M) from SE000013500(1U_0201_10V6M) . 5.Change JSPK1 part to SP02000HC10(8pin) from SP020019S00(6pin) . Add location RA67(10K_0402_5%) pull high to +3.3V_RUN. Add JSPK1.6 net SMART_SPK_DET1# connect to GPP_C22.	0.2 (X01)
27	66	2018/08/09	Modified according to GPIO map v1.4	Delete net NFC_ACTIVITY_STATUS#. Change RZ1473 pin1 to NC. Change netname to PTP_DISABLE# from TP_DISABLE#. Change netname to PTP_DISABLE#_R from TP_DISABLE#_R.	0.2 (X01)
28	9	2018/08/09	Modified according to GPIO map v1.4	Add GPP_C22 net SMART_SPK_DET1# connect to JSPK1.6.	0.2 (X01)
29	77	2018/08/09	Modified Semi-circular screw holes footprint	Change H26,H7,H6,H25,H9,H24,H23,H22 footprint to H_xPxN(NPTH) .	0.2 (X01)
30	58	2018/08/20	Modified layout Limit height problem	Change QE2 part to SB000014X00 from SB00000PV00.	0.2 (X01)
31	66	2018/08/20	Modified layout Limit height problem	Change QZ18 part to SB000017J00 from SB00001FT00.	0.2 (X01)
32	11	2018/08/20	CMOS1 PAD 蓋綠漆	Change CMOS1 footprint to SHORTPADS-NPM from SHORTPADS.	0.2 (X01)
33	11	2018/08/20	Modified parts according to Intel MOW WW30	Change CC96 part to SE00000M000(22U_0603_6.3V6M) from SE000001120(22U_0805_6.3V6M) [0805 part shortage]. Change CC96 to pop from depop.	0.2 (X01)
34	09	2018/08/20	Modified CNV DT topology series resistor value according to Intel MOW WW32	Change RC710,RC711 part to SD028330A80(33_0402_5%) from SD028750A80(75_0402_5%) .	0.2 (X01)
35	23	2018/08/20	Modified layout Limit height problem	Change CD17 part to SGA0000AM00(220U_D7_2V) from SGA00006A00(330U_D3_2.5V) .	0.2 (X01)
36	24	2018/08/20	Modified layout Limit height problem	Change CD49 part to SGA0000AM00(220U_D7_2V) from SGA00006A00(330U_D3_2.5V) .	0.2 (X01)
37	59	2018/08/20	Modified Board ID resistor to X01	Change RE79 part to SD028130380(130K_0402_5%) from SD028240380(240K_0402_5%) .	0.2 (X01)
38	52	2018/08/20	Modified parts according to RF request	Change CZ227~CZ230 part to SE071121J80(120P_0402_50V8J) from SE071101J80(100P_0402_50V8J) . Change CZ227~CZ230 to pop from depop. Change CZ307,CZ308 part to SE174270J80(27P_0201_25V8J) from SE000011F00(100P_0201_25V7K) . Change CZ307,CZ308 to pop from depop. Add location CZ233,CZ234 SE174101J80(100P_0201_25V8J) .	0.2 (X01)
39	50	2018/08/20	Modified parts to NPO capacitance	Change CT359 part to SE174101J80(100P_0201_25V8J) from SE000011F00(100P_0201_25V7K) .	0.2 (X01)
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40	24	2018/08/22	Modified parts according to ESD request	Add location DD1(SCA00002A00).	0.2 (X01)
41	70	2018/08/22	Modified parts to correct capacitance voltage	Change CR15,CR22 part to SE00000UC00(1U_0201_6.3V6M) from SE000013500(1U_0201_10V6M).	0.2 (X01)
42	58	2018/08/22	Add RTC(coin battery) voltage detect circuit	Delete location T143 test point. Change EC side GPIO011 pin netname to RTC_DET# from GPIO011. Add offpage RTC_DET#.	0.2 (X01)
43	58	2018/08/23	1.Fixed power sequence EA request 2.Modified RTC(coin battery) voltage detect circuit	1.Change RE361 pin 2 net connection to 1.0V_PRIM_PWRGD from 1.8V_PRIM_PWRGD. 2.Add location RE401 SD043100280(10K_0201_5%) pull up to +1.8V_PRIM_VTR3.	0.2 (X01)
44	70	2018/08/23	Fixed double net problem	Delete net SDWP_Q.	0.2 (X01)
45	78	2018/08/23	Fixed double net problem	Delete net +3.3V_SSD_UZ53.	0.2 (X01)
46	01	2018/08/23	Add Motherboard DPN(PWB)	Add Merion14 PWB DD1CY.	0.2 (X01)
47	66	2018/08/24	Modified parts according to ESD request	Add location DZ14,DZ15(SC300001Y00).	0.2 (X01)
48	66	2018/08/27	1.Delete Semi-circular screw hole 2.Delete unnecessary screw hole	1.Delete location H26,H7,H6,H25,H9,H24,H23,H22. 2.Delete location H19.	0.2 (X01)
49	38	2018/08/27	Update EDP connector symbol	Update JEDP1 connector symbol.	0.2 (X01)
50	52	2018/08/27	Update 4x4 Antenna connectors symbol	Update JANT1,JANT2 connectors symbol.	0.2 (X01)
51	52	2018/08/27	Modified JSPK1 pin define to correct routing	Swap JSPK1 pin define(1 to 8,2 to 7...).	0.2 (X01)
52	58	2018/08/28	Modified SSD_SCP# pull up to reserved	Change location RE821 to depop from pop.	0.2 (X01)
53	78	2018/08/31	1.Fixed power sequence EA request 2.Modified WLAN_PWR_EN pull up power rail according to Intel recommend 3.Delete unnecessary parts, align with X10 projects	1.Change CZ113 part to SE071101J80(100P_0402_50V8J) from SE074471K80(470P_0402_50V7K). 2.Add location RZ1483 SD028200280(20K_0402_5%) pull up to +3.3V_ALW. Change RZ379 to depop from pop. 3.Delete reserved location RZ375(20K_0402_5%).	0.2 (X01)
54	01	2018/08/31	Modified Motherboard DPN(PWB) according to PJE request	Change Merion14 PWB to 7YM2P from DD1CY.	0.2 (X01)
55	68	2018/08/31	1.Modified M.2 2280 Power Decoupling for support Intel Teton Glacier 2.Delete unnecessary parts, align with X10 projects	1.Change CN61,CN62 part to SE102104K0(0.1U_0402_10V7K) from SE00000SV00(0.1U_0201_10V6K). Add location CN79,CN80,CN81,CN82,CN84 SE076103K80(0.01U_0402_16V7K). Add location CN86 SE102104K00(0.1U_0402_10V7K). Add location CN87 SE00000M000(22U_0603_6.3V6M). 2.Delete location RN125~RN128,RN77,RN78,RN81,RN82(0_0201_5%).	0.2 (X01)
56	79	2018/08/31	Delete unnecessary parts, align with X10 projects	Delete reserved location RE375(0_0201_5%). Delete location RE560(0_0201_5%).	0.2 (X01)
57	11	2018/08/31	Delete unnecessary parts, align with X10 projects	Delete location RC740(0_0201_5%). Delete net PCH_PLTRST#_EC.	0.2 (X01)
58	66	2018/08/31	Delete unnecessary parts, align with X10 projects	Delete location RZ87(0_0201_5%). Delete reserved location DZ7(SCS00006300). Change RZ1473 to depop from pop.	0.2 (X01)
59	56	2018/08/31	Modified location to correct	Change location CA78 to CA29. Change location CA79 to CA49.	0.2 (X01)
60	52	2018/09/03	JSIM1 footprint change to use 2nd source footprint	Change JSIM1 footprint to TAISO_159-1000300600 from JAE_SF51S006V4DR1000Q.	0.2 (X01)
61	09	2018/09/04	Modified CNV_RGI_DT pull up follow Intel RVP	Change RC842 part to SD028200280(20K_0402_5%) from SD028100280(10K_0402_5%).	0.2 (X01)
62	08	2018/09/04	Modified GPP_C2 pull up follow Intel RVP	Change RC266 part to SD028470180(4.7K_0402_5%) from SD028220180(2.2K_0402_5%).	0.2 (X01)
63	38	2018/09/05	Reserved FUSE package location	Change RZ1387,RV100 to SD00000ZS00(0.01_0603_1%) from SD00000XJ00(0.01_0805_1%). Add location RZ98,RV103 SD00000ZS00(0.01_0603_1%).(footprint is FUSE SP040007G00)	0.2 (X01)
64	58	2018/09/07	Modified FPR pull up power rail	Change RE706~RE709 pull up power rail to +3.3V_FPBTN from +3.3V_RUN.	0.2 (X01)
65	38	2018/09/11	Modified part according to sourcer request	Change CV15 part to SE00000G880(0.1U_0402_25V6) from SE074104K80(0.1U_0402_50V7K).	0.2 (X01)
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66	79	2018/10/31	1.Modified M-BIST circuit for DC mode LED flash issue 2.Modified part according to sourcer request	1.Change CZ218 part to SE00000X880(2.2U_0201_6.3V6M) from SE00000UC00(1U_0201_6.3V6M) 2.Chane CZ218 part to SE000008880(2.2U_0402_6.3V6M) from SE00000X880(2.2U_0201_6.3V6M)	0.3 (X02)	
67	56	2018/10/31	Modified part according to sourcer request	Chane CA35 part to SE000008880(2.2U_0402_6.3V6M) from SE00000X880(2.2U_0201_6.3V6M)	0.3 (X02)	
68	59	2018/10/31	1.Modified part according to sourcer request 2.Modified Board ID resistor to X02	1.Chane CE12 part to SE000008880(2.2U_0402_6.3V6M) from SE00000X880(2.2U_0201_6.3V6M) 2.Change RE79 part to SD028620280(62K_0402_5%) from SD028130380(130K_0402_5%)	0.3 (X02)	
69	38	2018/10/31	1.Add Fuse part,modified location 2.Modified part to reserved Fuse location 3.Modified CAM,Touch Fuse	1.Change location RV100 to FV1,RV103 to FV2,RZ98 to FZ1,RZ1387 to FZ2. Change RV100,RV103,RZ98,RZ1387 part to SP040007G00(Fuse 1A_0603) 2.Change RZ1476 part to SD013000080(0_0603_5%) from SD028000080(0_0402_5%) 3.Change FZ1,FV2 part to SP040007F00(Fuse 0.5A_0603) from SP040007G00(Fuse 1A_0603)	0.3 (X02)	
70	18	2018/10/31	Modified CPU BV23 pin power rail follow Intel RVP	Change CPU BV23 pin power rail to +3.3V_ALW_PCH from +3.3V_SPI	0.3 (X02)	
71	66	2018/10/31	Modified parts align with X10 projects	Change RZ10(100K_0402_5%) to pop from depop. Change RZ1414(0_0201_5%) to depop from pop	0.3 (X02)	
72	58	2018/10/31	Modified RTC_DET# net connection to PCH from EC side	Change RTC_DET# net connection to PCH side(GPP_D3) from EC side(GPIO011). Delete location RE401 pull up SD043100280(10K_0201_5%)	0.3 (X02)	
73	08	2018/10/31	Modified RTC_DET# net connection to PCH from EC side	Change RTC_DET# net connection to PCH side(GPP_D3) from EC side(GPIO011). Add location RC866 pull up SD043100280(10K_0201_5%)	0.3 (X02)	
74	64	2018/10/31	Modified part follow LED light test result	Change RZ32 to SD028100180(1K_0402_5%) from SD028330080(330_0402_5%)	0.3 (X02)	
75	52	2018/11/30	1.Modified parts shortage problem 2.Modified part according to RF request 3.Modified layout Limit height problem	1.Change QZ17 from SB00001GC00 to SB00001KM00 2.Change RZ1460(0_0201_5%) and RZ1461(0_0201_5%) from depop to pop 3.Change part CZ26 from SGA00005T00(H.max=1.9mm) to SGA00006800(H.max=1.1mm)	0.3 (X02)	
76	11	2018/12/06	Follow NB14 UU AR, follow Intel CNVi recommendation	Change RC237(100k_0402_5%) from depop to pop	0.3 (X02)	
77	52	2018/12/06	Follow NB14 UU AR, follow Intel CNVi recommendation	1.Add RZ603 CNV_BRI_PTX_DRX_R pull up(10k_0402_5%) to +1.8_PRIM for reserve 2.Delete location RZ371(0_0201_5%) and RZ81(0_0201_5%)	0.3 (X02)	
78	12	2018/12/06	Follow NB14 UU AR, follow Intel CNVi recommendation	1.Change RC752 from SD028750280(75k_0402_5%) to SD034715280(71.5k_0402_1%) 2.Change RC640 from SD034715280(71.5k_0402_1%) to SD028750280(75k_0402_5%)	0.3 (X02)	
79	13	2018/12/06	Follow NB14 UU AR, follow Intel CNVi recommendation	UC1.CR35 add test point(T423)	0.3 (X02)	
80	11	2018/12/11	Intel CNVi recommendation RC237 pop,But cold reset and global reset sequence timing fail,So depop RC237	Change RC237(100k_0402_5%) from pop to depop	0.3 (X02)	
81	52	2018/12/11	Add 4X4 WWAN netname	Add netname +2.7V_ANT_R connect to JNGFF2.20, +1.8v_ANT_R connect to JNGFF2.24	0.3 (X02)	
82	72	2018/12/11	Add CAP for reserve material shortage problem	Add CI103(150U_B2_6.3VM_R35M) reserve Co-layer with CI1(100U_A_6.3VM_R70M) material shortage problem	0.3 (X02)	
83	77	2018/12/13	Modified according to DFX request	Change CLIP1~CLIP12 form CLIP_0P6X7P0 to CLIP_0P8X7P0	0.3 (X02)	
84	52	2018/12/13	Modified according to RF request	1.Change CZ206 and CZ207 from depop to pop and change value from 100P to 27P 2.Add CZ311 and CZ312(27P_0402_50V8J) on +3.3V_WWAN for RF request	0.3 (X02)	
85	38	2018/12/13	Modified according to RF request	1.Add CZ313(27P_0201_25V8) on +LCDVDD for RF request 2.Add CZ314(27P_0402_50V8J) on +BL_PWR_SRC for RF request	0.3 (X02)	
86	64	2018/12/13	Modified according ME request	Change RZ28 from SD028330080(330_0402_5%) to SD028150080(150_0402_5%)	0.3 (X02)	
87	38	2018/12/17	Modified location to correct	1.Change Location from CZ313 to CV757 2.Change Location from CZ314 to CV758	0.3 (X02)	
88	9	2018/12/18	Reserve for MOV issue	Add RC867(0_0201_5%) reserve for BITS392123, can't play music after resume from CMS with headphone connected	0.3 (X02)	
89	12	2018/12/18	Follow spyglass, reserve for after global reset CNVI module lost issue	Add CNVI_EN# net connection to PCH side(GPP_H3), add RC868 PD(75K_0402_5%) for CNVI_EN#	0.3 (X02)	
90	52	2018/12/18	Follow spyglass, reserve for after global reset CNVI module lost issue	1.Add RZ827(0_0201_5%) connect to CNVI_EN# For reserve 2.Change net name from CNV_RF_RESET to CNV_DET#_EC	0.3 (X02)	
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